# Non-isolated Interleaved High Step-up Converter with Reduced Voltage Multiplier Stages and a Regenerative Turn-off Snubber 

Kazuhiro Umetani and Eiji Hiraki
Graduate School of Nature Science and Technology
Okayama University
Okayama, Japan

Masayoshi Yamamoto
Interdisciplinary Graduate School of Science and
Engineering
Shimane University
Matsue, Japan

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# Non-isolated Interleaved High Step-up Converter with Reduced Voltage Multiplier Stages and a Regenerative Turn-off Snubber 

Kazuhiro Umetani and Eiji Hiraki<br>Graduate School of Nature Science and Technology<br>Okayama University<br>Okayama, Japan<br>umetani@okayama-u.ac.jp

Masayoshi Yamamoto<br>Interdisciplinary Graduate School of Science and Engineering<br>Shimane University<br>Matsue, Japan


#### Abstract

This paper proposes a novel non-isolated high stepup converter suitable for miniaturization by high frequency design. High step-up converters with voltage multipliers are promising for high frequency design because many of them can be free from coupled inductors or transformers, which may lower the voltage gain due to the leakage inductance or may cause significant AC conduction loss in the primary winding. However, two issues can still hinder further miniaturization. One is that many multiplier stages may be needed to achieve extremely high voltage gain. The other is that high switching frequency may be restricted by severe turn-off voltage surge caused by high speed switching. The proposed converter addresses the former by applying a recently reported technique to a non-isolated boost converter. Additionally, the converter addresses the latter by proposing a simple passive regenerative turn-off snubber implementable only by two diodes and a capacitor. Experiments verified that the proposed converter achieves high voltage gain with fewer voltage multiplier stages compared to prior nonisolated high step-up converters. Additionally, the snubber successfully reduced the turn-off surge into half approximately without apparent deterioration of the efficiency.


Keywords-high step-up; voltage multiplier; interleaved boost converter; turn-off snubber; voltage surge

## I. Introduction

Recently, photovoltaic cells and fuel cells are attracting increasing attention as promising power sources with low environmental burden. These cells are generally stacked to enhance the voltage. However, highly stacked cells may often deteriorate the electric charge capacity because the worst cell with the least capacity tends to limit the capacity of the whole stack. To address the issue, high step-up converters can be applied to reduce the number of the stacked cells. Nonetheless, adding a converter will expand the volume. Therefore, high step-up converters are required to be miniaturized.

One basic strategy is high frequency design, i.e. to design a converter to operate at high switching frequency. However, basic converter topologies, such as the normal boost converter, the isolated flyback and forward converters, as well as the LLC converters [1]-[3], tend to have difficulties in achieving high voltage gain at high switching frequency.

The normal boost converter can suffer from severe switching loss due to large current and voltage stresses to the switching device. The isolated converters can suffer from decrease in the voltage gain because high frequency operation generally suppresses current induction in the secondary winding due to the leakage inductance. The LLC converter can suffer from large resonant current in the primary winding, causing large AC conduction loss particularly at high resonant frequency.

Except for these basic converters, a number of high step-up converter topologies have been proposed [4]-[21]. These topologies can be mainly classified into two categories according to the strategies towards high voltage gain.

One category utilizes coupled inductors or transformers [4]-[11]. This category is beneficial in achieving high voltage gain only by adding turns to the secondary winding. Additionally, many topologies of this category can employ voltage clamping capacitors to reduce voltage stress of the switching devices to a voltage far below the output voltage [4][11]. This generally suppresses the switching loss to alleviate the efficiency drop caused by high frequency operation. However, the leakage inductance may suppress the current induction in the secondary winding, or the large AC current in the primary winding may cause significant AC conduction loss, resulting in deterioration of the voltage gain particularly in high frequency operation.

The other category utilizes voltage multipliers or switchedcapacitor multipliers [12]-[21]. Many topologies of this category can be implemented by basic circuit components, such as inductors, capacitors, diodes, and switches. Hence, they can be free from coupled inductors and transformers. Additionally, many topologies [13]-[21] of this category can further reduce voltage stress of the switching devices to a voltage far below the output voltage, alleviating the efficiency drop by high frequency operation. Therefore, this category can be promising for miniaturization by high frequency design.

Nonetheless, this category still suffer from two difficulties: One is that high voltage gain can require many multiplier stages, thus hindering miniaturization; and the other is that severe turn-off voltage surge can appear because of high speed


Fig. 1. Proposed converters with 4 stages of a voltage multiplier.


Fig. 2. Operating waveforms of the basic topology of the proposed converter.
switching required for high frequency operation. As for the former difficulty, [20] has proposed a promising converter to reduce the multiplier stages. However, application of this converter is limited because it does not have common ground between the input and the output.

The purpose of this paper is to address these two difficulties. The former is addressed by improving the prior converter [20]; and the latter is addressed by proposing a novel passive


Fig. 3. Operating modes of the basic topology of the proposed converter.
regenerative turn-off snubber. As a result, this paper proposes a non-isolated high step-up converter with reduced voltage multiplier stages and the regenerative snubber. The snubber enables the switching devices to achieve the zero-voltage turnoff, thus suppressing the turn-off voltage surge. Certainly, the prior technique [20] already proposed an active clamp to suppress the surge. However, our snubber is beneficial in simple implementation because our snubber is composed of only three passive components, i.e. two diodes and a capacitor.

The following discussion is divided into three sections. Section II discusses the operational principles of the proposed converter theoretically. Section III presents experiments to confirm the operational principles. Finally, Section IV presents the conclusions.

## II. Proposed Converter

## A. Circuit Overview

Figure 1 illustrates the circuit topologies of the proposed converter. Figure 1(a) is the basic topology, configured as a two-phase interleaved boost converter with a voltage multiplier. This configuration is similar to the prior high stepup converter reported in [20]. However, the following two differences exist in the circuit topology: One is that rectifying diode D 9 is added so that this converter has common ground between the input and the output; and the other is that capacitor C1 is connected to switch S1 instead of switch S2. Capacitor C1 has the positive voltage on its terminal connected to capacitor C3, contrary to [20]. This difference enhances the voltage gain of the proposed converter slightly more than the prior converter, as shown later.

Figure 1(b) further incorporates the passive regenerative turn-off snubber composed of diodes Da1, Da2, and capacitor Ca . This snubber achieves zero-voltage turn-off of both S 1 and S2 without additional control algorithms of the switches. Diodes Da1 and Da2 can have small DC current rating because the current flows through the snubber only during the turn-off of S1 and S2. Snubber capacitor Ca also has much smaller capacitance compared to capacitors $\mathrm{C} 1-\mathrm{C} 8$ because Ca is used only to suppress rising speed of the drain voltage of S1 and S2 during their turn-off. Therefore, the proposed snubber can avoid adding significant volume.

## B. Operating Principles of the Proposed Converter

This subsection discusses the circuit behaviors of Fig. 1(a) to clarify the operating principles of the proposed converter.


Fig. 4. Operating waveforms of the proposed converter with the regenerative snubber.

The proposed converter operates similarly to the prior converter [20]. Operating waveforms are presented in Fig. 2. The on-state of S1 and S2 must overlap each other. Therefore, the switches are operated at duty cycles greater than 0.5 with 180 degree phase shift. Consequently, operation of the proposed converter consists of the following three modes presented in Fig. 3.

In mode A , both of the switches are in the on-state. The input voltage is applied to both inductors L1 and L2 to increase the current of the inductors.

In mode $\mathrm{B}, \mathrm{S} 1$ is in the off-state; and S 2 is in the on-state. The current of L1 flows through diodes D2, D4, D6, and D8 to charge C2, C4, C6, and C8. The current of L2 continues to increase, whereas the current of L1 decreases.

In mode $\mathrm{C}, \mathrm{S} 1$ is in the on-state; and S 2 is in the off-state. The current of L2 flows through diodes D1, D3, D5, and D7 to charge C1, C3, C5, and C7. At the same time, a part of the current of L2 flows through D9 to charge the output capacitor. The current of L1 continues to increase, whereas the current of L2 decreases.

## C. Regenerative Snubber

Next, this subsection discusses the circuit behavior of Fig. 1(b) to clarify the operating principles of the proposed regenerative snubber. The operation of Fig. 1(b) is similar to that of Fig 1(a). The operation consists of modes A-E. Modes A-C are the same as those of Fig. 1(a) because no current flows in the regenerative snubber. The regenerative snubber works in modes D and E , which are inserted between modes A and B and between modes A and C, respectively. Figure 4 shows the operation waveforms of the regenerative snubber. Figure 5 shows the current patterns in each mode. Hereafter, we explain the operation during modes D and E , respectively.

In mode $\mathrm{D}, \mathrm{S} 1$ is turned off and the current of L1 flows through Da 1 to charge Ca . Thus, rising of the drain voltage of S 1 is suppressed to reduce the turn-off voltage surge. Snubber capacitor Ca is entirely charged to the voltage $V_{\mathrm{C} 2}-V_{\mathrm{C} 1}$, where $V_{\mathrm{C} 1}$ and $V_{\mathrm{C} 2}$ are the voltage of C 1 and C 2 , respectively. Then, the current of L 1 flows through C 1 , entering mode B .


Fig. 5. Operating modes of the proposed converter with the regenerative snubber.

In mode E, S2 is turned off; and the current of L2 flows through Da 2 and C 1 to discharge Ca . Thus, rising of the drain voltage of S 2 is suppressed to reduce the turn-off voltage surge. After the drain voltage of S 2 rises to the voltage $V_{\mathrm{C}}$, the current flows to the voltage multiplier, entering mode C. Hence, the charge stored in Ca is discharged to C 1 and is finally regenerated as the output power. This indicates that the proposed snubber is regenerative; and therefore, it can suppress the energy loss caused by the snubber.

For effective zero-voltage turn-off, Ca should be entirely discharged to zero voltage before entering mode D ; and Ca should be charged to $V_{\mathrm{C} 1}$ before entering mode E . These two requirements can be met by achieving the relation $V_{\mathrm{C} 2}-V_{\mathrm{C} 1}=V_{\mathrm{C} 1}$. This relation requires the same duty cycle for S 1 and S 2 , as shown later. (This is shown by setting $D_{\mathrm{S} 1}$ and $D_{\mathrm{S} 2}$ at the same value in (10) and (11), where $D_{\mathrm{S} 1}$ and $D_{\mathrm{S} 2}$ are the duty cycles of S1 and S2, respectively.) Therefore, the proposed regenerative snubber needs the duty cycles of S1 and S2 to be set at almost same value.

## D. Voltage and Current in Steady Operation

This subsection analyzes the capacitor voltage and the inductor current in the steady operation based on the basic topology of the proposed converter. We generalize our discussion to cover the proposed converter with an N -stage voltage multiplier shown in Fig. 6. (Figure 1(a) corresponds to a special case with 4 stages.) For convenience, we assume that L1 and L2 have the same inductance $L$ and that all the capacitors in the voltage multiplier have the same capacitance C. Furthermore, we assume that the voltage ripple of $\mathrm{C} 1-$ $\mathrm{C}(2 N)$ is ignorable, as well as the current ripple of L1 and L2. We denote the capacitor voltage as ' $V$ ' with subscript of the capacitor index, and the diode current during mode B or C (either mode in which the current flows through this diode) as ' $I$ ' with subscript of the diode index.


Fig. 6. Basic topology of the proposed converter with an $N$-stage voltage ultiplier.

According to the current flow of mode B shown in Fig. 3, we have the following relation between the average current through L1 $\left(I_{\mathrm{L} 1}\right)$ and the diode current:

$$
\begin{equation*}
I_{\mathrm{L} 1}=I_{\mathrm{D} 2}+I_{\mathrm{D} 4}+\cdots+I_{\mathrm{D}(2 N)} . \tag{1}
\end{equation*}
$$

Similarly, according to mode C , we have the relation between the average current through L2 ( $I_{\mathrm{L} 2}$ ) and the diode current:

$$
\begin{equation*}
I_{L 2}=I_{\mathrm{D} 1}+I_{\mathrm{D} 3}+\cdots+I_{\mathrm{D}(2 N-1)}+I_{\mathrm{D}(2 N+1)} . \tag{2}
\end{equation*}
$$

First, we focus on the average voltage of the capacitors. Equating the total current flow into a capacitor with the time derivative of the average charge in the capacitor, we obtain (3) and (4) for the capacitors $\mathrm{C}(2 k-1)$ and $\mathrm{C}(2 k)$, where $k$ is an arbitrary natural number from 1 to $N$.

$$
\begin{gather*}
C \frac{d V_{\mathrm{C}(2 k-1)}}{d t}=-\left(1-D_{\mathrm{S} 1}\right)^{N-k+1} I_{n=1} I_{\mathrm{D}(2 N+2-2 n)}+\left(1-D_{\mathrm{S} 2}\right)^{N-k+1} \sum_{n=1} I_{\mathrm{D}(2 N+1-2 n)}  \tag{3}\\
C \frac{d V_{\mathrm{C}(2 k)}}{d t}=\left(1-D_{\mathrm{S} 1}\right)^{N-k+1} I_{\mathrm{D}(2 N+2-2 n)}-\left(1-D_{\mathrm{S} 2}\right) \sum_{n=1}^{N-k+1} I_{\mathrm{D}(2 N+3-2 n)} \tag{4}
\end{gather*}
$$

where $D_{\mathrm{S} 1}$ and $D_{\mathrm{S} 2}$ are duty cycles of S 1 and S 2 , respectively.

In steady operation, all time derivative terms must vanish. Hence, we obtain the solution of (3) and (4) for the steady operation, using (1) and (2):

$$
\begin{equation*}
I_{\mathrm{D} 1}=I_{\mathrm{D} 3}=\cdots=I_{\mathrm{D}(2 N-1)}=I_{\mathrm{D}(2 N+1)}=\frac{I_{L 2}}{N+1}, \tag{5}
\end{equation*}
$$

$$
\begin{equation*}
I_{\mathrm{D} 2}=I_{\mathrm{D} 4}=\cdots=I_{\mathrm{D}(2 N)}=\frac{I_{\mathrm{L} 1}}{N} \tag{6}
\end{equation*}
$$

$$
\begin{equation*}
\left(1-D_{\mathrm{s} 2}\right) \frac{I_{\mathrm{L} 2}}{N+1}=\left(1-D_{\mathrm{S} 1}\right) \frac{I_{\mathrm{L} 1}}{N} \tag{7}
\end{equation*}
$$

According to (5) and (7), the output current $I_{\text {OUT }}$ can be expressed as

$$
\begin{equation*}
I_{\mathrm{OUT}}=\left(1-D_{\mathrm{S} 2}\right) I_{D(2 N+1)}=\left(1-D_{\mathrm{S} 2}\right) \frac{I_{\mathrm{L} 2}}{N+1}=\left(1-D_{\mathrm{S} 1}\right) \frac{I_{\mathrm{L} 1}}{N} . \tag{8}
\end{equation*}
$$

Next, we investigate the time derivative of the average current through L1 and L2. The drain voltage of S1 in mode B is equal to $V_{\mathrm{C} 2}-V_{\mathrm{C} 1}$; and the drain voltage of S 2 in mode C is equal to $V_{\mathrm{Cl}}$. Hence, we obtain

$$
\begin{gather*}
L \frac{d I_{\mathrm{L} 1}}{d t}=D_{\mathrm{S} 1} V_{\mathrm{IN}}-\left(1-D_{\mathrm{S} 1}\right)\left(V_{\mathrm{C} 2}-V_{\mathrm{C} 1}-V_{\mathrm{IN}}\right)  \tag{9}\\
L \frac{d I_{\mathrm{L} 2}}{d t}=D_{\mathrm{S} 2} V_{\mathrm{IN}}-\left(1-D_{\mathrm{S} 2}\right)\left(V_{\mathrm{C} 1}-V_{\mathrm{IN}}\right) \tag{10}
\end{gather*}
$$

where $V_{\text {IN }}$ is the input voltage. The voltage relations in the steady operation can be obtained by regarding all time derivative as zero in (9) and (10). As a result, we have

$$
\begin{equation*}
V_{\mathrm{C} 1}=\frac{V_{\mathrm{IN}}}{1-D_{\mathrm{S} 2}} \tag{11}
\end{equation*}
$$

$$
\begin{equation*}
V_{\mathrm{C} 2}=\left(\frac{1}{1-D_{\mathrm{S} 1}}+\frac{1}{1-D_{\mathrm{S} 2}}\right) V_{\mathrm{IN}} . \tag{12}
\end{equation*}
$$

Equations (5) and (6) indicate that all the diodes conduct current in either modes B or C in the steady operation. In mode B , diodes $\mathrm{D} 2, \mathrm{D} 4, \ldots, \mathrm{D}(2 N)$ conduct current to connect capacitors C3, C5, $\ldots, \mathrm{C}(2 N-1)$ in parallel to capacitors C4, C6, $\ldots, \mathrm{C}(2 N)$, respectively. Similarly, in mode C, diodes D1, D3, $\ldots, \mathrm{D}(2 N-1)$ conduct current to connect capacitors $\mathrm{C} 2, \mathrm{C} 4, \ldots$, $\mathrm{C}(2 N-2)$ in parallel to capacitors $\mathrm{C} 3, \mathrm{C} 5, \ldots, \mathrm{C}(2 N-1)$, respectively. Hence, the capacitor voltage of $\mathrm{C} 2-\mathrm{C}(2 N)$ must be the same. As a result, we have

$$
\begin{equation*}
V_{\mathrm{C} 2}=V_{\mathrm{C} 3}=\cdots=V_{\mathrm{C}(2 N)}=\left(\frac{1}{1-D_{\mathrm{S} 1}}+\frac{1}{1-D_{\mathrm{S} 2}}\right) V_{\mathrm{IN}} . \tag{13}
\end{equation*}
$$

As mentioned in Subsection II.C, the proposed regenerative snubber needs $V_{\mathrm{C} 2}-V_{\mathrm{C} 1}=V_{\mathrm{C} 1}$. This requirement can be met by setting $D_{\mathrm{S} 1}$ and $D_{\mathrm{S} 2}$ at the same duty cycle $D$ in (11) and (12). In this case, the voltage of the capacitors can be expressed as

$$
\begin{equation*}
V_{\mathrm{C} 1}=\frac{1}{1-D} V_{\mathrm{IN}}, \quad V_{\mathrm{C} 2}=V_{\mathrm{C} 3}=\cdots=V_{\mathrm{C}(2 N)}=\frac{2}{1-D} V_{\mathrm{IN}} . \tag{14}
\end{equation*}
$$

## E. Voltage Gain

The output voltage $V_{\text {OUT }}$ is equal to the voltage potential of the positive terminal of $\mathrm{C}(2 N)$ in mode C , if we neglect the forward voltage drop at the diodes. Consequently, the voltage gain $G$ is obtained as

$$
\begin{equation*}
G=\frac{N}{1-D_{\mathrm{S} 1}}+\frac{N+1}{1-D_{\mathrm{s} 2}} \tag{15}
\end{equation*}
$$

This result is consistent with the energy conservation. In fact, we obtain the following relation from (8) and (15), if we denote the input current as $I_{\mathrm{IN}}$ :

$$
\begin{align*}
& I_{\mathrm{L} 1}=\frac{N}{1-D_{\mathrm{S} 1}} I_{\mathrm{OUT}}, \quad I_{\mathrm{L} 2}=\frac{N+1}{1-D_{\mathrm{S} 2}} I_{\mathrm{OUT}} .  \tag{16}\\
& \therefore I_{\mathrm{IN}}=I_{\mathrm{L} 1}+I_{\mathrm{L} 2}=G I_{\mathrm{OUT}} .
\end{align*}
$$

Therefore, as expected, the input energy is equal to the output energy in the steady operation because $I_{\text {IN }} V_{\text {IN }}=I_{\text {OUT }} V_{\text {OUT }}$.

If we set $D_{\mathrm{S} 1}$ and $D_{\mathrm{S} 2}$ at the same duty cycle $D$, the voltage gain $G$ can be expressed as

$$
\begin{equation*}
G=\frac{2 N+1}{1-D} \tag{17}
\end{equation*}
$$

As we have seen above, the proposed converter offers slightly larger voltage gain by $1 /(1-D)$ compared to the prior converter [20]. This voltage gain is obtained not merely by adding $\mathrm{D}(2 N+1)$ to the prior converter because the maximum voltage potential in the prior converter is smaller than the output voltage of the proposed converter by $V_{\mathrm{IN}} /(1-D)$. In fact, the voltage potential of the positive terminal of capacitor $\mathrm{C}(2 N)$ is enhanced by $V_{\mathrm{C} 1}$ during mode C in the proposed converter owing to capacitor C 1 . Therefore, the difference in the voltage gain is contributed not only by adding diode $\mathrm{D}(2 N+1)$ but also by placing C1 in series with S1.

Compared to the prior non-isolated converters with multistage voltage multipliers [14], [16]-[18], which have common ground between the input and the output, the proposed converter greatly reduces the number of the voltage multiplier stages. The voltage gain of these prior converters can be expressed as $(N+1) /(1-D)$ or $N /(1-D)$. Therefore, if $N$ is set at a large number, the proposed converter can reduce the stages into half approximately.

## F. Voltage Stress of the Switches

Next, we analyze the voltage stress $V_{\mathrm{S} 1}$ and $V_{\mathrm{S} 2}$ of S 1 and S2 during their off-state. According to the current flow in modes B and C shown in Fig. 3, $V_{\mathrm{S} 1}$ and $V_{\mathrm{S} 2}$ are obtained using (11) and (12):

$$
\begin{equation*}
V_{\mathrm{S} 1}=V_{\mathrm{C} 2}-V_{\mathrm{C} 1}=\frac{V_{\mathrm{IN}}}{\left(1-D_{\mathrm{S} 1}\right)}, \quad V_{\mathrm{S} 2}=V_{\mathrm{C} 1}=\frac{V_{\mathrm{IN}}}{\left(1-D_{\mathrm{S} 2}\right)} . \tag{18}
\end{equation*}
$$


$\begin{array}{lll}\text { (a) R. Gules et al. (2003) [14] } & \text { (b) M. Prudente et al. (2008) [16] }\end{array}$

(c) J. C. Rosas-Caro et al. (2008) [17]

(d) S. V. Araújo et al. (2008) [18]

Fig. 7. Prior converters employed for comparison of the circuit elements.

TABLE I. COMPARISON OF THE CIRCUIT ELEMENTS.

|  | Proposed <br> Converter <br> (Fig. 1(a)) | Fig. 7(a) | Fig. 7(b) | Fig. 7(c) | Fig. 7(d) |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  | Number of <br> elements | 8 | 16 | 16 | 17 |
| Max. <br> Voltage [V] | 89 | 44 | 356 | 44 | 44 |
| DiodeNumber of <br> elements | 9 | 18 | 17 | 17 | 18 |
| Max. <br> Voltage [V] | 89 | 89 | 44 | 44 | 89 |
| SwitchNumber of <br> elements | 2 | 2 | 1 | 1 | 2 |
| Max. <br> Voltage [V] | 44 | 44 | 44 | 44 | 44 |
| InductorNumber of <br> elements | 2 | 2 | 9 | 1 | 2 |

$\dagger$ The output voltage and the duty cycle are 400 V and $75 \%$, respectively.
$\neq$ The input and output smoothing capacitors are not included in this table.
This result indicates that the voltage stress is far smaller than the output voltage $V_{\text {OUT. }}$. In fact, if we assume the same duty cycle for S 1 and S 2 , the ratios of the voltage stress to $V_{\text {OUT }}$ are obtained from (17) and (18) as

$$
\begin{equation*}
\frac{V_{\mathrm{S} 1}}{V_{\mathrm{OUT}}}=\frac{V_{\mathrm{S} 2}}{V_{\mathrm{oUT}}}=\frac{1}{2 N+1} \tag{19}
\end{equation*}
$$



Fig. 8. Prototype of the proposed converter with the regenerative snubber. (Capacitor Ca is mounted on the bottom side.)

TABLE II. SPECIFICATIONS OF THE PROTOTYPES

| Input Voltage | 11 V (approx.) |
| :---: | :---: |
| Max. Output Voltage | 400 V |
| Max. Output Power | 90 W |
| Switching Frequency | 200 kHz |
| Gating Voltage | 10 V |
| L1, L2 | 27 uH (Sagami 7G14A-270M) |
| S1, S2 | FDP52N20 (Fairchild) |
| D1-D8, Dt, Ds1, Ds2 | ES3DB-13-F (Diodes Zetex) |
| C1-C8 | 1 uF (Murata GRM55DR72E105KW01L) |
| Cs | 3 nF (Murata GRM21AR72E332KW01D) |

## G. Comparison of the Circuit Elements

As we have seen above, the proposed converter can reduce the voltage multiplier stages. This reduces the number of the circuit elements, which can lead to miniaturization of the converter. The purpose of this subsection is to estimate the reduction effect of circuit elements in comparison with the prior non-isolated converters with multi-stage voltage multipliers.

Figure 7 shows the prior non-isolated converters for comparison, reported in [14], [16]-[18]. (The converter reported in [20] is not included because this converter does not have common ground with the input and the output.) These prior converters are all designed to achieve the voltage gain of 36 at the same duty cycle of $75 \%$. (All switches are assumed to operate at the same duty cycle.) In order to calculate the voltage stress of the circuit elements, we set the maximum output voltage at 400 V .

Table I shows comparison of the number of the circuit elements, as well as their maximum voltage stress. The result reveals that the proposed converter reduces the number of capacitors and diodes approximately into half, owing to reduction in the voltage multiplier stages. On the other hand, the voltage stress of the capacitors and diodes are doubled compared to the prior converters. Therefore, if increase in the voltage stress does not lead to significant increase in the


Fig. 9. Relation between the voltage gain and the duty cycle in the proposed converter. The same duty cycle was set for S1 and S2.


Fig. 10. Voltage and current waveforms of the proposed converter without the snubber. The output was set at $400 \mathrm{~V}, 75 \mathrm{~W}$. Measurement points P1-P4, PS1, and PS2 are shown in Fig. 1(a).
volume of the circuit elements, the proposed converter can effectively miniaturize high step-up converters.
III. EXPERIMENT

## A. Prototypes

In order to verify the operating principles of the proposed converter, we tested two prototypes: One has the configuration of Fig. 1(a), and the other has the configuration of Fig. 1(b). Figure 8 shows the photograph of the prototype of Fig. 1(b). Table II shows the specifications of the prototypes. Switches S1 and S2 were operated at the same duty cycle. The switching frequency was set at 200 kHz .


Fig. 11. Comparison of the rising speed of the drain voltage at the turn-off between with and without the snubber. (The output was set at $400 \mathrm{~V}, 75 \mathrm{~W}$.)

## B. Voltage gain

Figure 9 shows the dependency of the voltage gain on the duty cycle. The input was set at $11 \mathrm{~V}, 75 \mathrm{~W}$; and the duty cycle was varied from $5 \%$ to $80 \%$. Accordingly, the output voltage was changed from 200 V to 500 V .

The results were found to agree well with the theoretical voltage gain calculated according to (17). In fact, the theory predicted the experimental voltage gain within an error of $5 \%$.

## C. Operating Waveforms of the Proposed Converter

Figure 10 shows the voltage and current waveforms of the prototype without the regenerative snubber, when the output was set at $400 \mathrm{~V}, 75 \mathrm{~W}$. The voltage waveforms were measured at the points P1-P4, PS1, and PS2 shown in Fig. 1(a). The duty cycle was set at $75 \%$.

The result revealed that the voltage waveforms were consistent with the theory. According to (14), we expected that $V_{\mathrm{C} 1}$ is equal to 44 V and $V_{\mathrm{C} 2}-V_{\mathrm{C} 8}$ are equal to 89 V . The experimental waveforms were close to the theoretical values because the average voltage of $\mathrm{C} 1, \mathrm{C} 2, \mathrm{C} 3$ and C 4 were 48.1 V , $96.2 \mathrm{~V}, 92.4 \mathrm{~V}$, and 90.0 V , respectively. According to (19), we also expect that $V_{\mathrm{S} 1}$ and $V_{\mathrm{S} 2}$, i.e. the drain voltage of S 1 and S 2 during their off-state, are equal to 44 V . The experimental waveforms were also close to the theoretical value.

The current waveforms of the inductors L1 and L2 were also consistent with the theory. According to (7), we expected that the average current through L1 $\left(I_{\mathrm{L} 1}\right)$ is 0.8 times as large as the average current through L2 ( $I_{\mathrm{L} 2}$ ). The experimental

(a) without the snubber (Fig. 1(a))

(a) with the snubber (Fig. 1(b))

Fig. 12. Comparison of the turn-off voltage surge between with and without the proposed snubber. (The output was set at $400 \mathrm{~V}, 75 \mathrm{~W}$.)


Fig. 13. Comparison of the efficiency between with and without the proposed snubber. (The output was set at 400 V .)
waveform verified the theory because $I_{\mathrm{L} 1}$ and $I_{\mathrm{L} 2}$ were 3.4 A and 4.3 A , respectively.

## D. Turn-off Voltage Surge

Next, we compared the rising speed of the drain voltage at the turn-off between with and without the regenerative snubber to verify the operation principles of the snubber. The output was set at $400 \mathrm{~V}, 75 \mathrm{~W}$; and the duty cycle was set at $75 \%$. The results are presented in Fig. 11. The result indicates that the drain voltage of both S1 and S2 rose slowly at the turn-off in the prototype with the regenerative snubber. This result is consistent with the operation principles discussed in the previous section.

The turn-off voltage surge was also found to be suppressed in the prototype with the snubber. Figure 12 compares the drain voltage waveforms of S1 and S2 between with and without the
snubber. As a result, the voltage surge was successfully suppressed approximately into half in the prototype with the snubber.

## E. Efficiency

Figure 13 shows the experimental result of the efficiency of the prototypes, when the output was set at 400 V and the duty cycle was set at $75 \%$. As seen from the figure, the prototypes showed efficiency higher than $88 \%$.

According to the theory, the regenerative snubber achieves soft-switching at the turn-off of both S1 and S2. Hence, we expected improvement of the efficiency by the snubber. As a result, however, any apparent improvement was scarcely found in Fig. 13. The reason is not cleared in this paper. As a possible reason, reduction in the turn-off switching loss may be canceled by the conduction loss generated in the regenerative snubber. Nonetheless, it should be pointed out that the result does not negate usefulness of the proposed snubber because the snubber successfully reduced the turn-off voltage surge by small additional circuit without apparent reduction of the efficiency.

## IV. CONCLUSIONS

Photovoltaic cells and fuel cells often requires a small-sized high step-up converter in order to minimize the number of the stacked cells. This paper proposed a non-isolated high step-up converter with reduced voltage multiplier stages and a passive regenerative turn-off snubber as a promising candidate. The proposed converter has the following attractive features.

- High frequency design is easy because no coupled inductor nor transformer is used.
- Voltage stress of the switches can be far smaller than the output voltage.
- High voltage gain is achieved with fewer voltage multiplier stages compared with the prior non-isolated converter topologies.
- The turn-off voltage surge can be reduced by small passive additional circuit without apparent reduction of the efficiency.

Experimental results successfully verified the operating principles. The results support that the proposed converter is promising for applications of renewable energy sources.

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