Optimization of the balance between the gate-drain capacitance and the common source inductance for preventing the oscillatory false triggering of fast switching GaN-FETs

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Optimization of the Balance between the Gate-Drain Capacitance and the Common Source Inductance for Preventing the Oscillatory False Triggering of Fast Switching GaN-FETs

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***Abstract*—GaN-FETs are attractive switching devices for their fast switching capability. However, they often suffer from the oscillatory false triggering, i.e. a series of self-sustaining repetitive false triggering induced after a fast switching. The purpose of this paper is to derive a design instruction to prevent this phenomenon. According to the previous study, the oscillatory false triggering was found to be caused by a parasitic oscillator circuit formed of a GaN-FET, its parasitic capacitance, and the parasitic inductance of the wiring. This paper analyzed the oscillatory condition to elucidate the design requirement to prevent the oscillatory false triggering. As a result, balancing the gate-drain parasitic capacitance and the common source inductance to achieve an appropriate ratio was found to be essential for preventing the oscillatory false triggering. Experiment successfully supported prevention of this phenomenon by balancing these two factors.**

Keywords—common source inductance; false triggering; GaN-FET; switching; oscillatory condition

I. INTRODUCTION

The Gallium Nitride Field Effect Transistors (GaN-FETs) are attracting attention as next generation switching devices. Owing to their low on-state resistance and fast switching capability [1][2], GaN-FETs are expected to greatly contribute to miniaturization and efficiency improvement of power converters. However, GaN-FETs are reported to be susceptible to false triggering [3]–[5], such as self-turn-on [6], because of the low gate threshold voltage and large switching noise caused by the fast switching. Particularly, GaN-FETs are reported to cause the oscillatory false triggering, which is a self-sustaining uncontrollable series of repetitive false triggering after a fast switching [7]–[9]. In this phenomenon, the turn-ons and the turn-offs repeat at a far higher frequency than the switching frequency; and furthermore, they often last during far longer period than the switching transient time. Because this oscillatory false triggering can cause enormous switching loss, it may be a severe issue for applying GaN-FETs to industrial applications.

As for the normal false triggering without self-sustaining repetition, the common source inductance [9]–[13], or the parasitic inductance of the source terminal, is known to play an important role [14]–[16]; and therefore, minimizing this inductance is pointed out to be effective for prevention of the false triggering [17][18]. However, this approach may not be effective for the oscillatory false triggering, because the oscillatory false triggering is reported to have different mechanism from the normal false triggering [7][8].

According to [7][8], the oscillatory false triggering can be explained as the oscillation caused by a parasitic oscillator circuit formed of the three elements: the GaN-FET, its parasitic capacitance, and the parasitic inductance of the wiring. Fast transient of the drain current at the switching excites this oscillator, resulting in the self-sustaining repetitive false triggering. This explanation implies the existence of a design instruction of the parasitic inductance to prevent the oscillatory false triggering because the oscillatory condition may be avoided by design optimization of the parasitic inductance.

The purpose of this paper is to give a design instruction to prevent the oscillatory false triggering based on the oscillatory condition of the parasitic oscillator circuit. Certainly, [8] discussed the oscillatory condition based on an analytical model of the parasitic oscillator circuit. As a result, [8] elucidated that the parasitic inductance of the wiring should be designed so that the parasitic resonance in the gating circuit should have the frequency far apart from the parasitic resonance of the power circuit.

However, many GaN-FET applications may have difficulty in design optimization of the parasitic resonance frequencies of the gating and power circuits. According to [8], large difference is required between these two resonance frequencies to prevent the oscillation, if these parasitic resonances have high Q factors. Therefore, large difference will be required, when the gate resistance is minimized to achieve fast switching or the parasitic resistance of the wiring is reduced as a consequence of minimization of the parasitic inductance, as is often the cases in GaN-FET applications. On the other hand, the parasitic inductance of the gating and power circuits tends to have the same order of value as a result of shortening the wiring to

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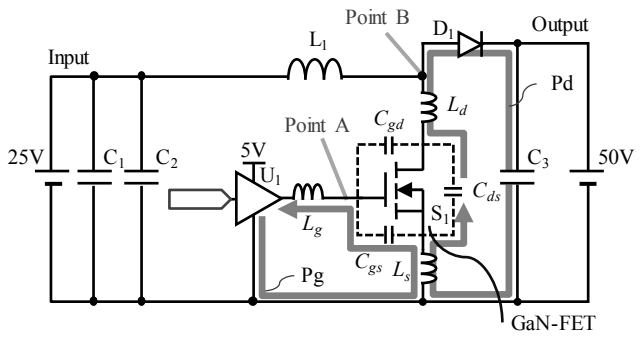

Fig. 1. Circuit diagram of the experimental boost chopper.

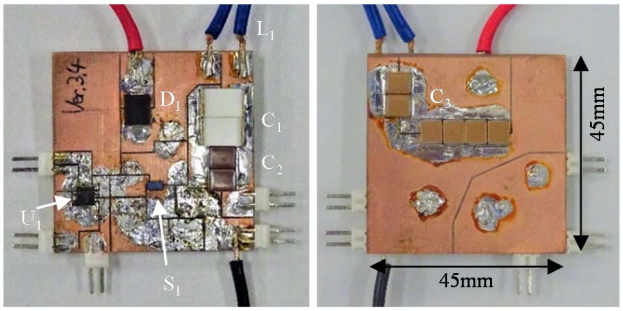

Fig. 2. Photographs of the experimental chopper.

TABLE I. LIST OF CIRCUIT ELEMENTS IN EXPERIMENTAL CHOPPER

S_1	GaN-FET EPC2010 (EPC Corp.)
D_1	Si-SBD SK4200L (Micro Commercial Components)
C_1	Film capacitor 1nF×2pcs ECWU1105KCV (Panasonic)
C_2	Ceramic capacitor 22uF×2pcs CKG57NX7S2A226M500JH (TDK Corp.)
C_3	Ceramic capacitor 2.2μF×6pcs CKG57KX7T2E225M335JH (TDK Corp.)
L_1	Inductor 27μF×4pcs 7G14A-270M (Sagami)
U_1	Driver LM5113SDE/NOPB (Texas Instruments)

minimize the parasitic inductance of the power circuit for suppression of the switching surge. Hence, the parasitic resonance frequencies of the gating and power circuits tend to have similar resonance frequencies because the gate-source capacitance and the drain-source capacitance also tend to have the same order of value in many switching devices. Therefore, designing sufficient difference in the resonant frequencies will be possibly difficult in GaN-FET applications.

As we have seen, the analysis of [8] implied possible difficulty in preventing the oscillatory false triggering for GaN-FET applications. However, it is worth noting that the preceding analysis [7][8] on the oscillatory false triggering neglected the common source inductance, although this inductance is widely known to play an important role in normal false triggering. Therefore, it seems natural to suppose that the oscillatory false triggering is also deeply affected by the common source inductance.

Generally, the different analytical model of the parasitic oscillator circuit results in different oscillatory conditions. Hence, another oscillatory condition may be obtained by including the common source inductance into the analytical model of the oscillatory false triggering. This implies a possibility to find another more convenient design instruction by considering the common source inductance.

Based on this idea, this paper derives a novel design instruction for preventing the oscillatory false triggering by considering the common source inductance. Certainly, considering the common source inductance generally requires extremely complicated analysis to solve the oscillatory condition. However, in order to simplify our discussion, we rather neglect the gate resistance as well as the parasitic resistance of the wiring from the analytical model of the oscillatory false triggering. This corresponds to the worst case of the extremely fast switching using GaN-FETs, because these resistances generally damp the parasitic resonance and contribute to suppression of the occurrence of the parasitic oscillation, i.e. the oscillatory false triggering. Therefore, this analytical model of the worst case will offer the sufficient condition for preventing the parasitic oscillation, which can be utilized as a universal design instruction for preventing the oscillatory false triggering.

The following discussion consists of 4 sections. Section II presents a brief review of the oscillatory false triggering based on the experimental waveforms observed in the experimental boost chopper of a GaN-FET and a Si-SBD. Then, Section III constructs the analytical model of the oscillatory false triggering and theoretically investigates the oscillatory condition. As a result, this section derives the sufficient condition for preventing the oscillatory false triggering and interpret this condition as a novel design instruction. Section IV carries out an experiment to verify the effectiveness of this design instruction. Finally, section V gives conclusions.

II. OSCILLATORY FALSE TRIGGERING

This section reports the oscillatory false triggering observed in an experimental boost chopper. Figures 1 and 2 show the circuit diagram and the photographs of the chopper. Table shows the list of the circuit elements. The experimental boost chopper consists of a GaN-FET and a Si-SBD. Capacitance C_{gd}, C_{gs}, and C_{ds} are the parasitic capacitance of S_1. The loop wiring paths Pg and Pd are the AC current paths of the gating and power circuits, respectively. Pg forms a loop wiring path from the gate to the source of S_1 through the gate driver, whereas Pd forms a loop wiring path from the drain to the source of S_1 through diode D_1 and output capacitor C_3. The inductance L_s is the common source inductance, which is the inductance of the common path shared by Pg and Pd, measured as L_s=0.6nH. The inductance L_g and L_d are the parasitic inductance of the loop wiring paths Pg and Pd except for the common source path, measured as L_g=8.0nH and L_d =7.6nH, respectively. (Detailed measurement method of L_s, L_g, and L_d is presented in the appendix.)

In order to observe switching waveforms of a single turn-off, the boost chopper was operated for only one switching cycle. At first, the GaN-FET S_1 was kept at the on-state for 32μs. Then, S_1 was turned off to observe the oscillatory false triggering after the switching.

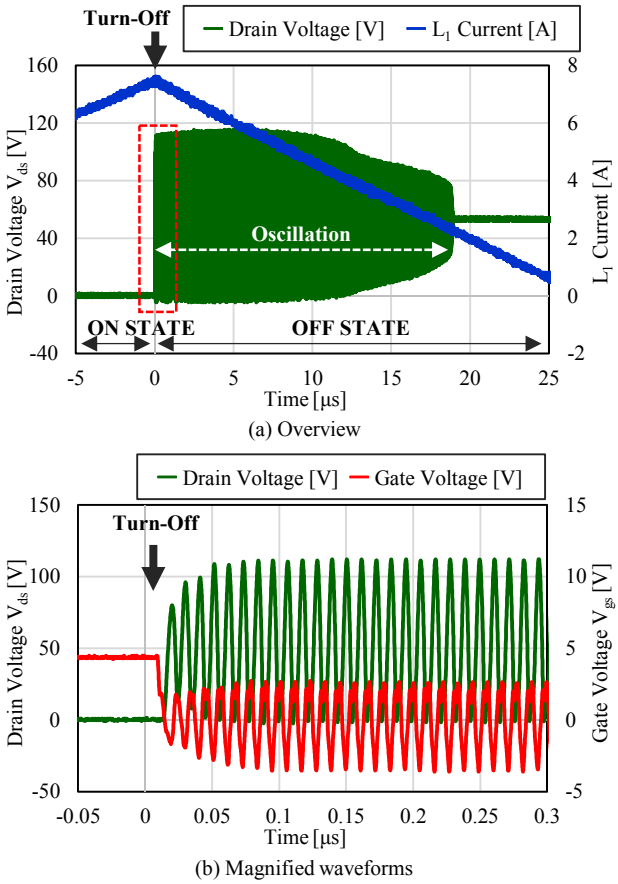

Fig. 3. Experimental waveforms after the turn off.

Figure 3 shows the results. Figure 3(a) shows that the oscillation was excited and lasted for 18μs in the drain voltage of S_1 after the turn-off. Figure 3(b) shows the magnified voltage waveforms of the drain and the gate of S_1 just after the turn-off. As can be seen from the figure, the gate voltage repetitively crossed the S_1 threshold voltage of 1.4V due to the self-sustaining oscillation. Furthermore, the drain voltage dropped at the rise of the gate voltage, indicating that the oscillation is composed of repetitive false triggering. This repetitive false triggering had far larger frequency than the commonly utilized switching frequencies. According to Fig. 3(b), the frequency of the repetitive false triggering was found to be 90MHz approximately. These features are consistent with the oscillatory false triggering reported in [8].

Figure 3 implies generation of the enormous switching loss due to the uncontrollable self-sustaining oscillation of repetitive false triggering. This fact indicates that the oscillatory false triggering can be a severe obstacle for practical application of GaN-FETs; and therefore, derivation of the practical design instruction is intensely required to avoid the oscillatory false triggering.

III. Design Instruction to Prevent the Oscillatory False Triggering

A. Model Construction

According to the previous study [7][8], the oscillatory false triggering can be explained as the oscillation induced by the parasitic oscillator. This section investigates the oscillatory condition of the parasitic oscillator to derive a design instruction for preventing the oscillatory false triggering.

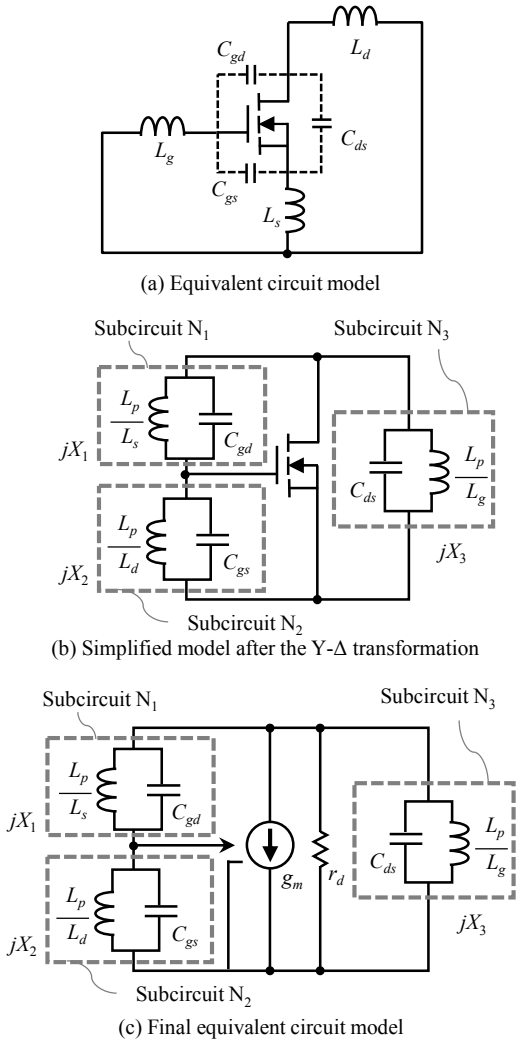

Fig. 4. Analytical models of the oscillatory false triggering.

First, we construct the parasitic oscillator model based on Fig. 1. Because the oscillatory false triggering has the extremely high frequency, C_1–C_3 can be regarded as short-circuit; and, L_1 can be regarded as open circuit. During the off-state of S_1, the DC current flows in D_1. Therefore, D_1 can also be regarded as short-circuit. Furthermore, as mentioned in the introduction, the parasitic resistance as well as the gate resistance is neglected in the analysis in order to seek for a design instruction applicable even to an extremely fast switching, in which the length of the wiring of the power circuit is minimized for suppressing the switching surge and the gate resistance is minimized for faster gate drive. As a result, the equivalent circuit model for the oscillatory false triggering is obtained as shown in Fig. 4(a).

The equivalent circuit Fig. 4(a) is, however, complicated for circuit analysis. Therefore, this equivalent circuit is transformed into a simple circuit model in advance. For this purpose, the Y-Δ transformation is applied to the Y-shaped network of L_g, L_d,

and L_s in Fig. 4(a). As a result, we obtain Fig. 4(b). Inductance L_p in Fig. 4(b) is defined as

$$L_p = L_s L_g + L_g L_d + L_d L_s. \tag{1}$$

Finally, switching device S_1 is modeled for the analysis. Generally, the electrical characteristics of the switching devices are highly non-linear. However, we model S_1 by a simple linear model with a voltage-controlled current source and the drain-source resistance. As we have seen in the previous section, the oscillation in the gate voltage waveform in Fig. 3 has the same frequency as that in the drain voltage waveform. Therefore, it seems to be natural to suppose that the oscillatory false triggering can be modeled by a linear model, similarly as in [8]. As a result, we obtain the final equivalent circuit shown in Fig. 4(c). The mutual conductance of the voltage-controlled current source and the resistance of the drain-source resistance are denoted as g_m and r_d, respectively.

B. Analysis of the Oscillatory Condition

Next, Fig. 4(c) is analyzed to investigate the oscillatory condition. Note that Fig. 4(c) has a form of a Barkhausen-type oscillator. The oscillatory condition of Fig. 4(c) can be easily obtained using the Barkhausen criterion [19]. According to this criterion, the oscillation occurs, if the real part of the open-loop gain H is greater than the unity, i.e. $\mathrm{Re}(H)\geq 1$ at the frequency at which the imaginary part of H is zero, i.e. $\mathrm{Im}(H)=0$. If the reactance of subcircuits N_1–N_3 are denoted as X_1–X_3, respectively, the open-loop gain H of Fig. 4(c) is obtained as

$$\begin{aligned} H &= -g_m \{r_d \,//\, j(X_1+X_2) \,//\, jX_3\} \frac{X_2}{X_1+X_2} \\ &= -\frac{jg_m r_d X_2 X_3}{j(X_1+X_2)X_3 + r_d(X_1+X_2+X_3)}. \end{aligned} \tag{2}$$

Therefore, the open-loop gain H meets the Barkhausen criterion, if the following relations are satisfied:

$$X_1 + X_2 + X_3 = 0, \tag{3}$$

$$-\frac{g_m r_d X_2}{X_1 + X_2} \geq 1. \tag{4}$$

The first relation, i.e. (3), is called as the frequency condition, whereas the latter, i.e. (4), is called as the gain condition.

Commonly, $g_m r_d$ of switching devices tends to take a large value. Hence, we assume that $g_m r_d$ is infinitely large positive value in order to simplify the discussion. In addition, we also assume that $|X_1|$ is far greater than $|X_2|$ because C_{gd} is commonly far smaller than C_{gs} and L_p/L_s is commonly far greater than L_p/L_d. Under these assumptions, the frequency and gain conditions can be reduced into a simpler equivalent condition. As a result, the Barkhausen criterion can be reduced into the following condition: At the frequency at which $X_1+X_2+X_3=0$, the polarity of X_1, X_2, and X_3 should satisfy either

1. X_2 and X_3 are both positive and X_1 is negative; or,
2. X_2 and X_3 are both negative and X_1 is positive.

Note that subcircuits N_1–N_3 are parallel-connected LC resonators in Fig. 4(c). Therefore, the polarity of their reactance is positive, if the frequency is below the resonance frequency; and the polarity is negative, if the frequency is above the resonance frequency.

Let f_1–f_3 be the resonance frequencies of N_1–N_3, respectively. Then, we can find 6 possible magnitude relations among f_1–f_3 as illustrated in Fig. 5. This figure indicates that only the following two relations can avoid the aforementioned condition on the polarity of X_1, X_2, and X_3 at any frequency region:

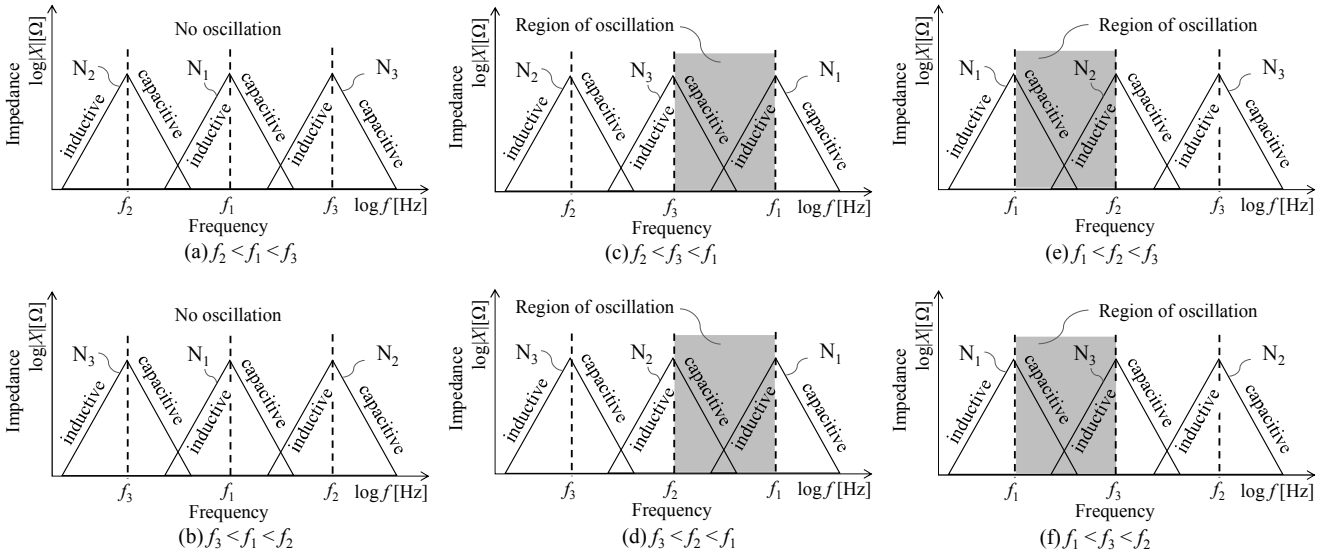

Fig. 5. Relation between the frequency region of the oscillation and the order of resonance frequencies f_1–f_3. The vertical axis is the impedance of subcircuits N_1–N_3; and the horizontal axis is the frequency.

$$f_2 < f_1 < f_3, \quad f_3 < f_1 < f_2. \tag{5}$$

Therefore, the Barkhausen criterion is not satisfied under (5); and therefore, the oscillation does not occur.

As for the other cases, i.e. $f_2<f_3<f_1$, $f_3<f_2<f_1$, $f_1<f_2<f_3$, and $f_1<f_3<f_2$, there exists a frequency region that satisfies the aforementioned condition on the polarity of X_1, X_2, and X_3. (This frequency region is shadowed in Fig. 5.) Note that X_1+X_3 takes an extremely large negative value at the lowest frequency of the shadowed region, whereas X_1+X_3 takes an extremely large positive value at the highest frequency of the shadowed region. Therefore, there exists a frequency within the shadowed region at which $X_1+X_2+X_3$ takes zero. As a result, the oscillation occurs in all the cases of $f_2<f_3<f_1$, $f_3<f_2<f_1$, $f_1<f_2<f_3$, and $f_1<f_3<f_2$.

To summarize, the occurrence of the oscillation, i.e. the oscillatory false triggering, can be avoided, if f_1–f_3 are designed to satisfy (5). Noting that f_1–f_3 are defined as the resonance frequencies of subcircuits N_1–N_3, we can express these frequencies as

$$f_1 = \frac{1}{2\pi\sqrt{L_p C_{gd}/L_s}}, \quad f_2 = \frac{1}{2\pi\sqrt{L_p C_{gs}/L_d}}, \quad f_3 = \frac{1}{2\pi\sqrt{L_p C_{ds}/L_g}}. \tag{6}$$

Substituting (6) into (5), we finally obtain the condition of the parasitic inductance for preventing the oscillatory false triggering as

$$\frac{L_d}{C_{gs}} < \frac{L_s}{C_{gd}} < \frac{L_g}{C_{ds}} \quad \text{or} \quad \frac{L_g}{C_{ds}} < \frac{L_s}{C_{gd}} < \frac{L_d}{C_{gs}}. \tag{7}$$

This result indicates that the oscillatory false triggering can be prevented by designing L_s/C_{gd} within an appropriate range of value. This fact leads to a striking idea that too small L_s, as well as too large L_s, can cause the oscillatory false triggering. Consequently, this results suggests a novel design instruction that appropriate balance between L_s and C_{gd}, i.e. appropriate ratio of L_s and C_{gd}, should be designed to satisfy (7) in order to prevent the oscillatory false triggering.

Compared with the conventional design instruction presented in [8], this design instruction can be valid even if the frequency of the parasitic resonance of the gating circuit is close to that of the power circuit. According to the analysis of [8], the frequency of the parasitic resonance of the gate circuit (f_g) and the frequency of the parasitic resonance of the drain circuit (f_d) can be expressed as the following equation. (We approximate that C_{gd} is far smaller than C_{gs} and C_{ds}.)

$$f_g = \frac{1}{2\pi\sqrt{(L_g + L_s)C_{gs}}}, \quad f_d = \frac{1}{2\pi\sqrt{(L_d + L_s)C_{ds}}}. \tag{8}$$

Therefore, if we approximate as $L_g+L_s \approx L_g$ and $L_d+L_s \approx L_d$, (7) can be rewritten as

$$\frac{C_{gd}}{4\pi^2 C_{ds} C_{gs}} \frac{1}{f_d^2} < L_s < \frac{C_{gd}}{4\pi^2 C_{ds} C_{gs}} \frac{1}{f_g^2} \quad \text{or} \quad \frac{C_{gd}}{4\pi^2 C_{ds} C_{gs}} \frac{1}{f_g^2} < L_s < \frac{C_{gd}}{4\pi^2 C_{ds} C_{gs}} \frac{1}{f_d^2}. \tag{9}$$

Equation (9) indicates that the occurrence of the oscillatory false triggering can be prevented as far as L_s is designed to satisfy (9) even if f_g is close to f_d. Certainly, appropriate range of value for L_s is narrow under the condition in which f_g is close to f_d. However, appropriate design of L_s can be a universally applicable approach for preventing the oscillatory false triggering.

It is worth noting that the analysis of this section is targeted on the worst case, in which $g_m r_d$ is regarded to be infinitely large and the parasitic resistance, as well as the gate resistance, is regarded to be zero. Therefore, this design instruction can cover extremely high speed switching.

Certainly, actual power converters commonly contains parasitic resistance of the wiring as well as the gate resistance. Furthermore, the actual switching devices have finite $g_m r_d$. As a result, the Q factors of subcircuits N_1–N_3 are finite to damp the oscillation in actual power converters. In addition, the oscillatory condition (4) become more difficult to be satisfied under finite $g_m r_d$. As a consequence, the oscillatory false triggering may occur more rarely in actual power converters and the oscillatory false triggering may be prevented for wider range of L_s.

According to our discussion, we can also say that too small C_{gd} is not appropriate as well as too large C_{gd}. From the viewpoint of the oscillatory false triggering, C_{gd} should be designed to have appropriate range of value. However, this does not necessarily means that the effort to minimize C_{gd} is meaningless. As widely known, large C_{gd} may deteriorate the switching speed or cause the self-turn-on. Therefore, our design instruction, shown in (7), should be interpret that reduction only in C_{gd} or only L_s may be harmful and that both C_{gd} and L_s should be reduced to keep L_s/C_{gd} within an appropriate range of value.

IV. Experiment

An experiment was carried out to verify the effectiveness of the proposed design instruction, i.e. suppression of the occurrence of the oscillatory false triggering by designing the appropriate balance between C_{gd} and L_s. In this experiment, the experimental chopper shown in Section II was employed.

Figure 6 shows the PCB layout of this experimental chopper. This chopper is designed to be able to change the value of L_s by elongating or shortening the common source path, i.e. the AC current path shared by Pg and Pd. (Pg and Pd are the AC current paths of the gating circuit and the power circuit, respectively, defined in Fig. 1.) The common source path was changed by making a solder bridge on a selected point to connect the ground of the gating circuit to the source terminal of S_1. Figure 6 shows the six points for making the solder bridge to change L_s. In addition, further large L_s was implemented by cutting a part of the wiring path along the green line shown in Fig. 6. As a result, we obtained eight levels for L_s, and the range of L_s varied from

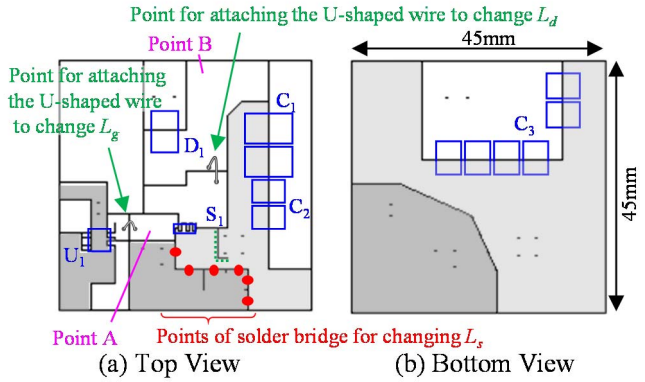

Fig. 6. Pattern layout of the experimental PCB.

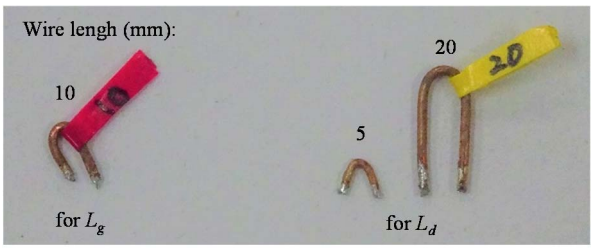

Fig. 7. Photograph of the U-shaped wires.

0.3nH to 1.9nH. The measurement method of L_s of the experimental chopper is described in the appendix.

In addition, the experimental chopper was designed to be able to change the value of L_g and L_d by elongating the gate and drain wiring using U-shaped wires. (The photograph of the U-shaped wires is shown in Fig. 7.) The length of the gate wiring was changed by selecting either attaching the 10mm U-shaped wire or making a solder bridge on the wiring path from the gate driver to the gate of S_1. On the other hand, the length of the drain wiring was changed by attaching either one of two U-shaped wires on the wiring path from the drain of S_1 to diode D_1. Certainly, the values of L_g and L_d were significantly affected not only by the U-shaped wires but also by the value selected for L_s because selection of L_s also leads to elongating and shortening of Pd and Pg. Hence, selecting the U-shaped wire only determines the range of L_g and L_d. We measured the values of L_g and L_d at each value of L_s, as shown in Table II. The measurement method of L_g and L_d of the experimental chopper is also described in the appendix.

In order to evaluate the effectiveness of the proposed design instruction, we designed L_g and L_d in this experiment so that the preceding design instruction [8] was not satisfied. Hence, the

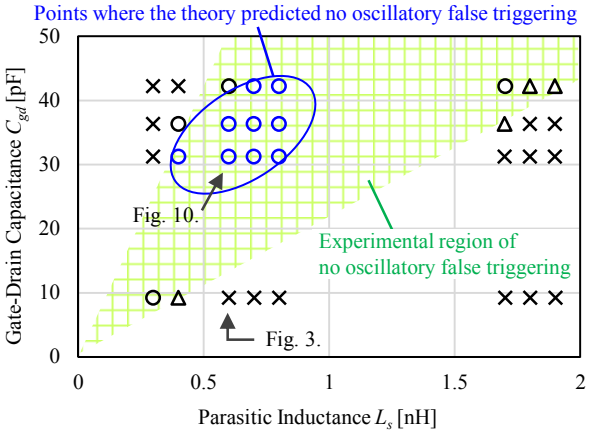

Fig. 8. Experimental result of occurrence of the oscillatory false triggering. L_g was the original gate wiring made with the solder bridge and L_d was implemented with the 5mm U-shaped wire. Blue marks indicates the points where the theory predicted non-occurrence of the oscillatory false triggering.

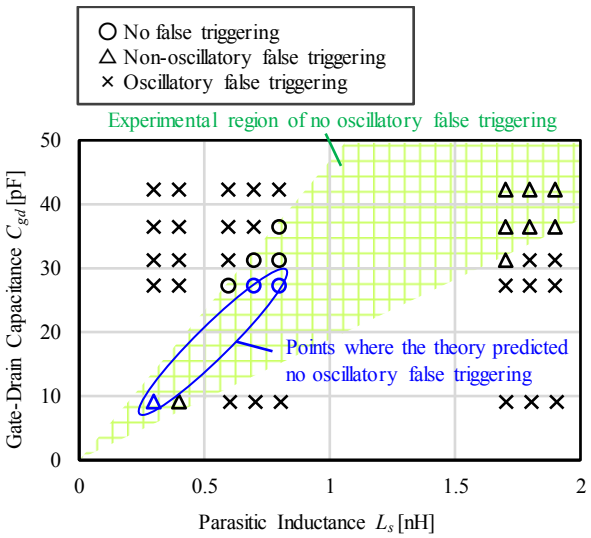

Fig. 9. Experimental result of occurrence of the oscillatory false triggering. L_g and L_d were implemented with the U-shaped wires 5mm and 20mm, respectively. Blue marks indicates the points where the theory predicted non-occurrence of the oscillatory false triggering.

parasitic resonance frequency f_g of the gating circuit was designed to be close to the resonant frequency f_d of the power circuit, according to the definition given as (8). Then, we set L_s at various values and observed the non-occurrence condition of the oscillatory false triggering.

TABLE II. INDUCTANCE VALUES FOR L_g AND L_d EMPLOYED IN THE EXPERIMENT

L_s [nH]		0.3	0.4	0.6	0.7	0.8	1.7	1.8	1.9
L_g [nH]	Solder bridge	5.3	6.4	8.0	10.0	11.7	10.2	11.5	12.4
	10mm wire	7.9	8.9	10.8	12.5	14.2	12.5	14.2	14.9
L_d [nH]	5mm wire	7.6	7.6	7.6	7.6	7.6	9.3	9.3	9.3
	20mm wire	14.2	14.2	14.2	14.2	14.2	15.9	15.9	15.9

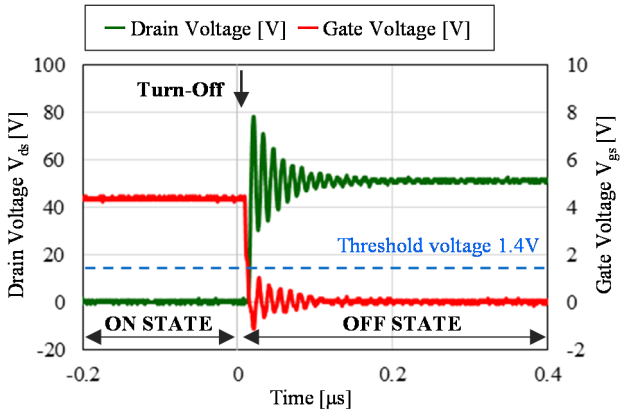

Fig. 10. Voltage waveforms at the turn-off when the oscillatory false triggering is suppressed.

In this experiment, we also evaluated the dependency of the non-occurrence condition on C_{gd}. For this purpose, we evaluated the range of L_s that prevents the oscillatory false triggering at five values of C_{gd}: 9.2pF, 27pF, 31pF, 36pF, and 42pF. The first value is the original capacitance of S_1, whereas the other values were implemented by adding a small-sized ceramic capacitor between the drain and gate terminals of S_1.

Figures 8 and 9 show the evaluation result of the non-occurrence condition of the oscillatory false triggering. In these figures, the repetitive false triggering more than ten times after the turn-off was judged as the oscillatory false triggering. The false triggering less than 10 times was classified as the non-oscillatory false triggering.

In Fig. 8, a solder bridge was made on the wiring path of the gate instead of the U-shaped wire; and the 5mm U-shaped wire is implemented on the wiring path of the drain. As a result, L_g and L_d were ranged 5.3–12.4nH and 7.6–9.3nH, respectively.

On the other hand, in Fig. 9, the 10mm U-shaped wire was attached on the wiring path of the gate; and the 20mm U-shaped wire was attached on the wiring path of the drain. As a result, L_g and L_d were ranged 7.9–14.9nH and 14.2–15.9nH, respectively.

As can be seen in Fig. 8 and Fig. 9, the oscillatory false triggering was suppressed in a certain range of L_s. In addition, this range shifted toward larger inductance as C_{gd} takes the larger capacitance. These features were consistent with the theoretical analysis. Furthermore, the experimentally observed region of the no false triggering was found to cover the theoretically predicted points, suggesting appropriateness of the theory.

Figures 8 and 9 indicate that too small L_s resulted in the oscillatory false triggering, similarly as too large L_s. This result implies that balancing L_s and C_{gd}, i.e. optimizing the ratio L_s/C_{gd}, is essential for preventing the oscillatory false triggering rather than simply minimizing L_s.

Figure 10 shows the switching waveform when the oscillatory false triggering was suppressed by setting L_s at 0.6nH and C_{gd} at 31pF, respectively. (L_g and L_d were set at 8.0nH and 7.6nH, respectively.) As can be seen in the figure, not only the oscillatory false triggering but also the normal false triggering disappeared in the switching waveform, suggesting practical effectiveness of the proposed design instruction.

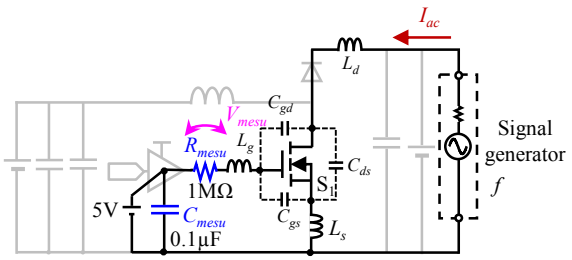

Fig. 11. Circuit diagram of the measurement method of the common source inductance.

V. Conclusions

The oscillatory false triggering has been reported to be a possible severe risk for industrial application of GaN-FETs. This paper addressed this issue by proposing a design instruction to prevent this phenomenon. This paper analyzed the occurrence condition of the oscillatory false triggering, considering the common source inductance as well as the other parasitic inductance of the wiring. The analysis revealed that the ratio of the gate-drain capacitance and the common source inductance is the key factor to be optimized for effective prevention of the oscillatory false triggering. Particularly, this analysis suggested that too small common source inductance can be harmful similarly as too large common source inductance, which may imply the necessity to optimize the common source inductance rather than to minimize the inductance.

Appendix

A. Measurement Method of Common Source Inductance L_s

In this experiment, a recently proposed measurement technique [12][13] was employed for the common source inductance. Figure 11 illustrates the measurement method. We employed another PCB with the same layout pattern as the experimental chopper. On this PCB, only the GaN-FET was mounted. We attached resistor R_{mesu} on the wiring path from the gate driver to the gate terminal of the GaN-FET. In addition, ceramic capacitor C_{mesu} was attached to connect the pads for the output terminal and the ground terminal of the gate driver. Then, we applied the DC voltage to C_{mesu} in order to keep the GaN-FET at the on-state. Finally, we connected the signal generator between the drain and the source of the GaN-FET to supply the high frequency sinusoidal AC current and measured the AC voltage across R_{mesu}.

As discussed in the preceding studies [12][13], the voltage induced at L_s appears at R_{mesu} because the resistance of R_{mesu} was designed to be far higher than the impedance of C_{gs} and L_g at the frequency of the sinusoidal AC current. Hence, L_s can be obtained using the following equation:

$$L_s = \frac{V_{mesu}}{2\pi f I_{ac}} \sin\phi, \tag{10}$$

where V_{mesu} and I_{ac} are the effective value of the voltage across R_{mesu} and the AC current supplied from the signal generator,

respectively; f is the frequency of the AC current; and ϕ is the phase difference between the voltage across R_{mesu} and the AC current.

We measured L_s by supplying the AC current of 0.2Ap at nine frequencies from 2MHz to 10MHz. Then, we averaged the results to determine L_s. Other parameters related to this measurement is presented in Fig. 11.

B. Measurement Method of Parasitic Inductance L_g and L_d

The inductance L_g and L_d are measured using the simple measurement method for the parasitic inductance of the loop wiring path [8]. In this method, we employed another PCB with the same layout pattern as the experimental chopper, similarly as in the previous subsection.

For the measurement of L_g, only a small surface-mount ceramic capacitor with the capacitance of C_{mg} was mounted on the pads for the GaN-FET to connect the gate and source terminals. In addition, we disposed a solder bridge to connect the pads of the output and ground terminals of the gate driver. As a result, the capacitor was short-circuited through the wiring of the gating circuit.

Then, we measured the frequency dependence of the impedance of this short-circuited capacitor. This short-circuited capacitor forms a parallel-connected LC resonator composed of the ceramic capacitor and the parasitic inductance L_g+L_s. Therefore, the resonance frequency can be measured based on the frequency of the peak impedance. If we denote the resonance frequency as f_{res}, L_g can be obtained as

$$L_g = \frac{1}{4\pi^2 f_{res}^2 C_{mg}} - L_s. \tag{11}$$

Similarly, for the measurement of L_d, we mounted a small surface-mount ceramic capacitor with the capacitance of C_{md} on the pads for the GaN-FET to connect the drain and source terminals. Then, we made solder bridges to connect the pads for diode D_1 and the pads for output capacitor C_3. As a result, the ceramic capacitor was short-circuited through the wiring of the power circuit. This short-circuited capacitor forms a parallel-connected LC resonator composed of the ceramic capacitor and the parasitic inductance L_d+L_s. Hence, by determining the resonance frequency as a result of the impedance measurement, we can obtain L_d as

$$L_d = \frac{1}{4\pi^2 f_{res}^2 C_{md}} - L_s. \tag{12}$$

In this experiment, we set both C_{mg} and C_{md} at 0.22uF.

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