# Practical Measurement Method for Parasitic Inductance in Wiring Networks of Multichip Power Modules


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***Abstract*—In recent years, multichip power modules (MCPMs) using SiC devices have been commercialized from the viewpoints of power conversion efficiency and heat dissipation performance. Wide bandgap (WBG) semiconductors such as SiC support fast switching but can cause parallel oscillations and high overshoot voltages. Equivalent circuit models are often used to analyze these problems, but modeling requires detailed parasitic inductances in the MCPM. Previous parasitic inductance measurement methods typically measured only loop inductance of the modules and often remain at the theoretical level without demonstration using actual MCPMs. To address these limitations, this paper proposes a measurement-based method that measures the parasitic inductance of branches on the equivalent circuit model as the mutual inductance between closed loops formed by the MCPM wiring structure, and also describes how this measurement can be implemented on actual MCPMs. Finally, the validity of the equivalent circuit model substituting the measured inductance is experimentally evaluated. This measurement method is more practical and is expected to be of great interest to MCPM layout designers.**



***Keywords— Parasitic Inductance, Multichip Power Modules, SiC-MOSFET***


## I. INTRODUCTION

In recent years, the commercialization of wide bandgap (WBG) semiconductors such as silicon carbide (SiC) has rapidly advanced. SiC MOSFETs offer superior characteristics such as high breakdown voltage and low on-resistance compared to conventional silicon based devices[1][2]. These advantages make them promising candidates for high-power applications, including electric vehicles and industrial motor drives.

In high power applications, multichip power modules (MCPMs) are commonly used due to their high power conversion efficiency and excellent thermal management[3]. MCPMs typically integrate multiple MOSFETs in parallel within a package that includes a baseplate for effective heat dissipation.

However, previous studies have reported that parallel-connected power modules using fast switching WBG devices suffer from parallel oscillation during switching events[4]-[7]. This raises concerns that similar phenomenon may occur in MCPMs. In this paper, the term parallel oscillation means the repeated amplification of switching noise that propagates among the parallel-connected MOSFETs, driven by their inherent amplification characteristics. This phenomenon results in increased ringing in the gate-source voltage, which can lead to sustained false turn-on. Such oscillations may cause significant switching losses and, in serious cases, lead to failure of the MCPM. Therefore, MCPM designers must implement an appropriate strategy to reduce this risk.

Equivalent circuit models of the high-side or low-side of a half-bridge are often used to analyze parallel oscillation by examining the resonance characteristics within the power module[5]-[7]. To construct such models, it is essential to accurately determine the internal parasitic impedance, including the parasitic inductance of each branch between current splitting points inside the power module.

Several previous studies have extracted parasitic inductances using simulation-based approaches[8][9]. These simulation-based extraction method offers a cost advantage because it does not require a physical prototype. However, accurate extraction requires detailed information about the internal structure of the MCPMs. Since the accuracy of the extracted results strongly depends not only on how precisely the internal structure is replicated but also on the validity of the analysis procedure, ensuring reliability remains a challenge. Therefore, a measurement-based method for extracting parasitic inductance is needed.

A previous study proposed a method to extract parasitic inductances based on an inductance matrix, focusing on closed loops formed by internal wiring structures of power modules[10]. Fig. 1 shows the equivalent circuit model of a parallel half-bridge module that includes parasitic inductances along the wiring paths. The proposed method defines multiple closed loops inside the power module, as shown in Fig. 1, and

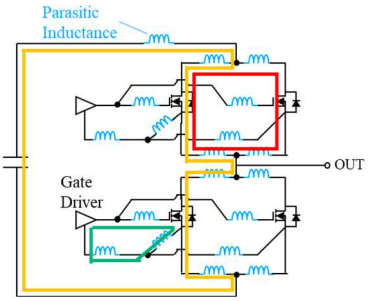



Fig. 1. Loop wiring formed within a parallel half-bridge power module

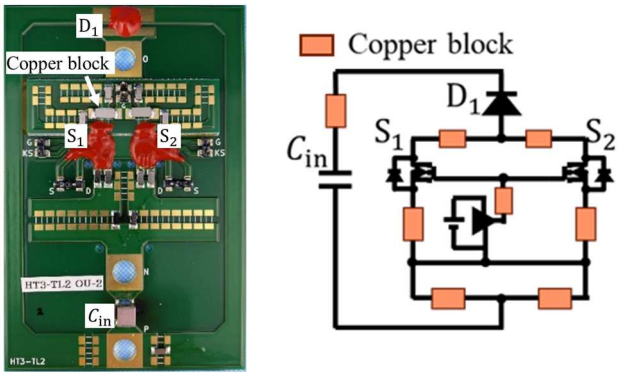
measures the inductance matrix between them. Then, the results are converted into effective inductances to construct the equivalent circuit model for circuit analysis. The inductance matrix includes magnetic coupling parameters between all internal wiring. Since the closed loops are defined based on actual current paths within the MCPM, the measured magnetic coupling inherently reflects the contribution of each branch. As a result, this approach allows for a theoretically consistent evaluation of the measurement results.

However, applying the proposed method to MCPMs with a large number of parallel-connected devices for high-power applications presents two major challenges.

The first challenge lies in the impracticality of exhaustively measuring all elements of the inductance matrix. For instance, when applying the proposed method to measure the parasitic inductances on the low-side of an MCPM with eight parallel-connected devices, the resulting inductance matrix becomes 22-dimensional, meaning that 484 elements must be measured. Furthermore, even if all elements could be measured, converting them into effective inductances becomes extremely complex as the matrix dimension increases.

The second challenge stems from the fact that the test circuit board used in prior research, shown in Fig. 2, was specifically designed to verify the measurement principle. As a result, the measurement procedure was not intended for practical MCPMs. Fig. 2(a) shows a photograph of the test board used in earlier study, while Fig. 2(b) shows its circuit diagram with copper blocks. To apply the proposed method, it is essential to form arbitrary closed loops within the MCPM using internal wiring. In the test circuit board, numerous land patterns were distributed across the surface, and attaching or detaching copper blocks allowed the formation of the required loops. However, commercial MCPMs don't have such a mechanism. In practice, the internal devices of the MCPM are interconnected via substrate traces, which makes it difficult to form arbitrary closed loops. Furthermore, since there are no easily accessible terminals inside MCPM package, it is difficult to connect measurement probes to inside of the MCPM. Therefore, a standardized measurement procedure is needed to ensure reliable implementation of the method in actual MCPMs.

In this paper, we propose a simplified and practical method for extracting parasitic inductance, building upon the closed loop based approach introduced in previous study[10]. The previous method requires constructing a full inductance




(a) Photograph of test circuit board

(b) Test circuit board schematic with copper blocks

Fig. 2. Test circuit board used to verify the measurement principle in a previous study[10]

matrix. However, the mutual inductance between distant wirings within the MCPM remains negligible due to eddy current effects induced by the baseplate. Therefore, not all elements of the inductance matrix contribute meaningfully to the circuit behavior. Based on this observation, the proposed method focuses only on the dominant magnetic coupling between nearby wires, which significantly reduces the number of required measurements.

The method starts by developing an equivalent circuit model based on the wiring network of the MCPM. Next, to measure the parasitic inductance of each branch, we define two closed loops that are constructed from internal wiring and share the branch. The parasitic inductance of the branch is then measured as the mutual inductance between these loops. Since the measurement involves injecting current into wires located near the target branch, the approach naturally accounts for magnetic coupling between neighboring paths. Furthermore, the proposed measurement procedure is independent of the specific interconnect layout of the MCPM, making it applicable even to complex and densely integrated modules.

This paper investigates the validity of the proposed measurement technique by applying it to the low-side parasitic inductances of a commercially available MCPM with an eight-parallel half-bridge configuration.

## II. Measurement Principle and Application to MCPM

This chapter first describes the measurement principle of the proposed method in Section A. Then, Section B to D explain how the method is applied to the MCPM investigated in this study.

### *A. Measurement Principle*

This section explains the measurement principle of the proposed method using Fig. 3. As a premise, a typical half-bridge power module allows the definition of closed loops formed by the wiring, as shown in Fig. 1. From the wiring network of power module, we extract two closed loop, $i$ and $j$, that share a branch, as illustrated in Fig. 3. In this paper, we measure the parasitic inductance of the branch commonly included in both loops as the mutual inductances between these loops. First, a high-frequency AC current $i_\mathrm{i}$ is injected into loop $i$, and the induced voltage $v_\mathrm{j}$ caused by $L$ is

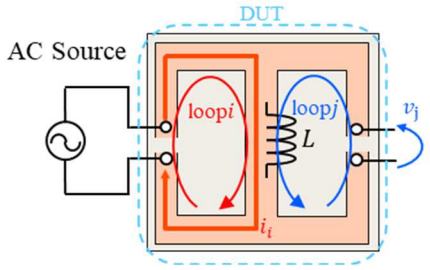



Fig. 3. Parasitic inductance measurement principle using two closed loops

measured in loop $j$. The parasitic inductance $L$ of the shared branch is calculated using (1), where $\theta$ is the phase difference between the current $i_i$, and the induced voltage $v_j$, and $\omega$ is the angular frequency.

$$L = M_{ij} = \frac{v_j}{\omega i_i} \sin\theta \tag{1}$$

Additionally, since the measurement applies current through the actual power module wiring in this measurement principle, measured parasitic inductance reflects magnetic coupling with nearby wiring.

### *B. Equivalent Circuit Modeling of the MCPM*

The investigated MCPM in this paper, is the commercially available BSM180D12P2E002 1.2 kV/ 204 A from ROHM. It is a half-bridge module with SiC MOSFETs. Fig. 4 shows a 3D model of the internal structure. Fig. 5 shows the wiring network on the low-side, where each MOSFET is connected via substrate traces and wire bonds. The equivalent circuit model is developed based on the wiring network shown in Fig. 5. The final equivalent circuit model is shown in Fig. 6, and its construction process is described below.

In this model, we first assign parasitic inductances to each branch of the network, neglecting spatially distributed inductance components. Note that the branches above the drain terminals are excluded, as the corresponding inductance inside each device is physically small and therefore considered negligible.

As mentioned in Chapter 1, mutual inductance between conductors that do not share a physical path is generally negligible. According to [11], the mutual inductance $M$ between parallel conductors, such as those shown in Fig. 7, can be calculated using (2). Based on this equation, Fig. 8 plots mutual inductance versus the distance between two conductors.

$$M \cong 2\times10^{-7} l \left[ \ln\left( \frac{l}{d} + \sqrt{\left(\frac{l}{d}\right)^2 + 1} \right) - \sqrt{1 + \left(\frac{d}{l}\right)^2} + \frac{d}{l} \right] \tag{2}$$

In the MCPM investigated in this paper(Fig. 4), the distance between devices is approximately 5 mm. From Fig. 8, it can be expected that the mutual inductance between such distant conductors within the MCPM is sufficiently small. Additionally, in actual layouts, the mutual inductance becomes even smaller due to angled placement of conductors

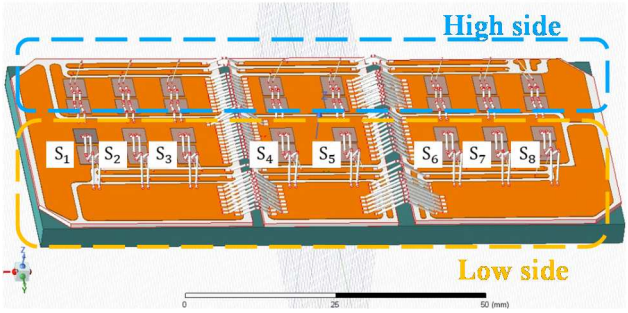



Fig. 4. 3D model of BSM180D12P2E002

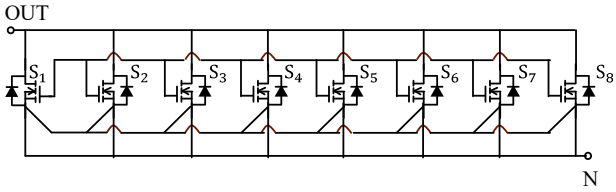



Fig. 5. Low side circuit network of Fig. 4

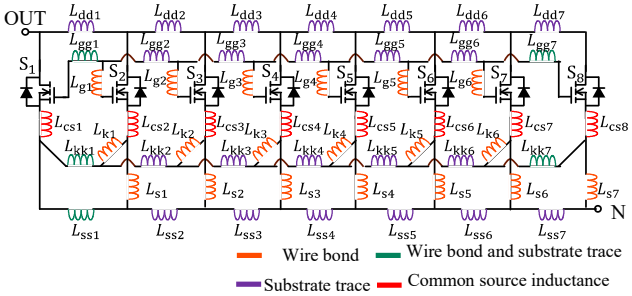



Fig. 6. Low side equivalent circuit model of Fig. 4

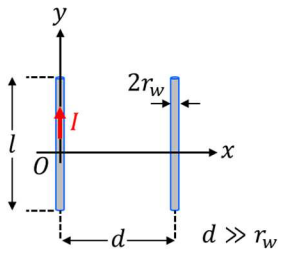



Fig. 7. Parallel two conductors

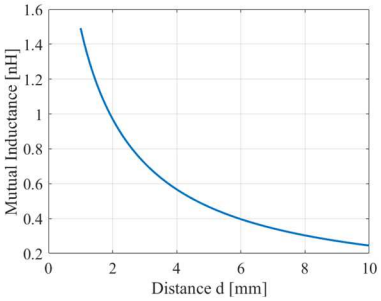



Fig. 8. Mutual inductance versus the distance between two conductors on Fig. 7

and eddy currents induced in the baseplate. Consequently, magnetic coupling between distant conductors is negligible.

However, we explicitly consider the common source inductance (CSI), which represents the magnetic coupling between the power and gate circuits. This is because CSI plays an important role in circuit operation [12][13]. In this study, we define the CSI as the mutual inductances between the wire bonds connected to the power-source and kelvin-source terminal, and apply a T-type equivalent circuit transformation to model it.

### C. Definition of Closed Loops for Investigated MCPM

As described in Section A, each parasitic inductance in Fig. 6 is measured as the mutual inductance between two closed loops that share the corresponding branch. The closed loop definitions are shown in Fig. 9. The closed loop $i_{\mathrm{p}}$ starts from the intermediate point terminal of the MCPM, passes through the drain-source of each device, and returns to the N terminal. The closed loop $i_{\mathrm{np}}$ connects the drain terminal and the power-source terminal of adjacent devices. The closed loop $i_{\mathrm{d}}$ connects the gate and drain terminals of adjacent devices. The closed loop $i_{\mathrm{g}}$ connects the gate and kelvin-source terminals of adjacent devices. The closed loop $i_{\mathrm{s}}$ connects the kelvin-source and power-source terminals of adjacent devices. Although omitted due to space limitations, these closed loops are actually defined in the same way for all eight parallel-connected devices.

During the measurement, we combine closed loops as shown in Fig. 3 for all branches indicated in Fig. 6 to perform the measurement. The combination of closed loops for measuring mutual inductance and the calculation procedure for each parasitic inductance in this paper are illustrated, as an example, using the parasitic inductance between $S_1$ and $S_2$ shown in Fig. 6, as described in equations (3) to (11). The same procedure is applied to the interconnections beyond $S_2$.

$$L_{\mathrm{dd1}} = M_{\mathrm{p2d1}} \tag{3}$$

$$L_{\mathrm{g1}} = M_{\mathrm{g1d2}} \tag{4}$$

$$L_{\mathrm{gg1}} = M_{\mathrm{d1g1}} - L_{\mathrm{g1}} \tag{5}$$

$$L_{\mathrm{cs1}} = M_{\mathrm{p1g1}} \tag{6}$$

$$L_{\mathrm{cs2}} = M_{\mathrm{p2g2}} \tag{7}$$

$$L_{\mathrm{k1}} = M_{\mathrm{g1s2}} \tag{8}$$

$$L_{\mathrm{kk1}} = M_{\mathrm{d1s1}} - L_{\mathrm{k1}} \tag{9}$$

$$L_{\mathrm{ss1}} = M_{\mathrm{p1np1}} - L_{\mathrm{cs1}} \tag{10}$$

$$L_{\mathrm{s1}} = M_{\mathrm{np1np2}} - L_{\mathrm{cs2}} \tag{11}$$

### D. Consideration for Closed Loop Combination

In the previous section, we described defined closed loops definition and the closed loop combinations used to measure each parasitic inductance shown in Fig. 6. However, in practical measurement, accurate results are difficult to obtain

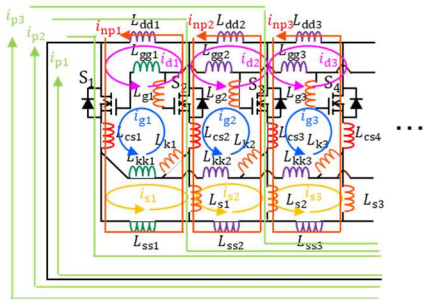



Fig. 9. Closed loop definition for parasitic inductance measurement

unless the combination of closed loops is appropriately selected. This section explains key considerations in parasitic inductance measurement, taking as an example the case of measuring the parasitic inductance $L_{\mathrm{s1}}$ shown in Fig. 6 associated with the power-source wire bond in device $S_2$, from the perspective of magnetic coupling between conductors.

The parasitic inductance $L_{\mathrm{s1}}$ can be obtained in two ways: by subtracting $L_{\mathrm{k1}}$ from the mutual inductance between $i_{\mathrm{s1}}$ and $i_{\mathrm{s2}}$, or by subtracting $L_{\mathrm{cs2}}$ from the mutual inductance between $i_{\mathrm{np1}}$ and $i_{\mathrm{np2}}$. Among these, using $i_{\mathrm{s1}}$ and $i_{\mathrm{s2}}$ path is particularly problematic. In general module, the power-source and kelvin-source wire bonds located in close proximity. When current flows through loop $i_{\mathrm{s1}}$ according to the principle in Fig. 3, strong magnetic coupling occurs between these two wire bonds. In actual circuit operation, the current in the gate wiring is much smaller than that in the main circuit, so the magnetic effect from the kelvin-source wire bond on the power-source wire bond is limited. However, when measuring the mutual inductance between $i_{\mathrm{s1}}$ and $i_{\mathrm{s2}}$, equal-magnitude current flows through both wire bonds, which causes the magnetic influence of the kelvin-source wire bond to become excessive. As a result, the measured inductance can significantly deviate from the actual parasitic inductance. Therefore, closed loops involving gate wiring should be avoided when measuring parasitic inductance on the power circuit.

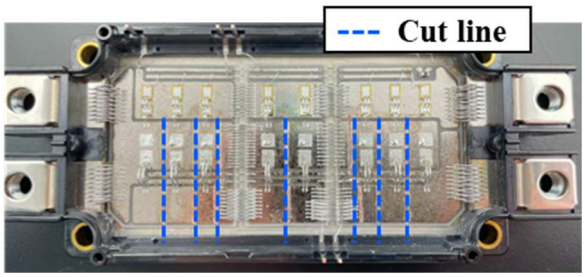
## III. Implementation of the Measurement Principle for a Commercial MCPM

In this chapter, we explain the two main challenges that arise when applying the measurement principle described in Chapter 2 to a commercial MCPM.

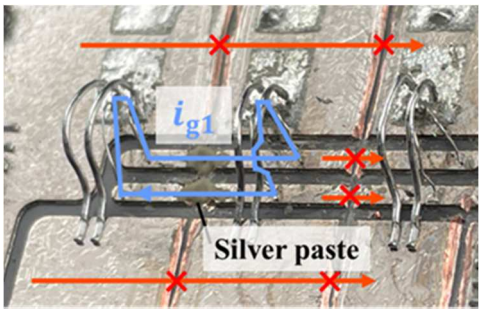
The first challenge is that the closed loops defined in Fig. 9 are not electrically independent within the MCPM. As a result, during the measurement process shown in Fig. 3, current may unintentionally flow through conductors outside the intended loop. This unintended current path prevents current from flowing only through the intended loop. As a result, measuring the desired parasitic inductance becomes difficult or even impossible.

To address this issue, this study introduces a method that involves physically cutting the substrate traces at positions where all the closed loops defined in Fig. 9 remain open, as shown in Fig. 10(a). During measurement, the necessary closed loop is reconstructed by reconnecting a portion of the cut trace using silver paste. Fig. 10(b) shows an example of

this process, where the closed loop $i_{g1}$ from Fig. 9 is formed. Silver paste is used instead of solder because the wide area of the substrate trace makes soldering difficult due to heat diffusion. Silver paste is uniformly applied to the cut section to form a reliable current path. Additionally, as shown in Fig. 10(a), both the semiconductor chips which have parasitic capacitance and the encapsulating gel which interferes with probe connection are removed. After removing the semiconductor chips, the wire bonds on the chips are cut at the position shown in Fig. 11 and then reconnected to the substrate traces using silver paste.




(a) Substrate trace cutting line




(b) Photograph showing the formation of closed loop $i_{g1}$

Fig. 10. Way of forming a closed loop on MCPM

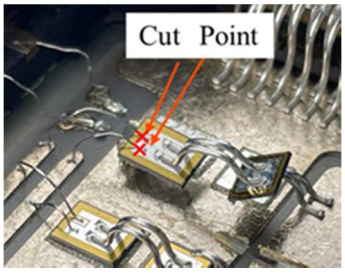



Fig. 11. Wire bond cutting point on bare chip

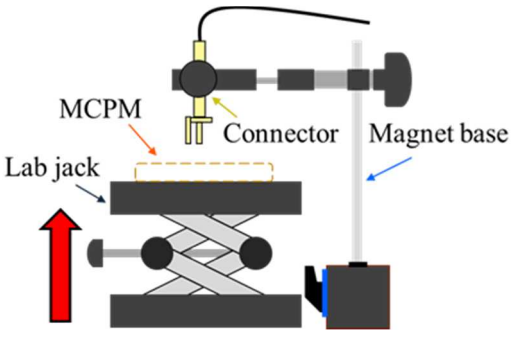



Fig. 12. Connector connection method to MCPM

The second challenge arises from the need to connect measurement probes directly to internal nodes of the MCPM when applying the measurement principle shown in Fig. 3. As previously mentioned, soldering inside the MCPM is impractical due to heat diffusion across the wide substrate traces, and bonding connectors with silver paste lacks sufficient mechanical strength for stable attachment.

To overcome this challenge, as shown in Fig. 12, we adopted a method in which an MMCX connector is fixed to a magnet base, and a lab jack is used to lift the MCPM until the connector contacts the designated substrate trace. Two contact points are established in this setup. One is used for injecting current into the MCPM, and the other is used for measuring the induced voltage. Although contact resistance occurs at the interface between the connector and the substrate trace, its influence is considered negligible in both cases. For the current injection point, the contact resistance is connected in series with the closed loop. Even if this resistance changes the current amplitude or its phase relative to the measured voltage, the parasitic inductance is still calculated based on equation (1), so the measurement is not affected. For the voltage measurement point, the input impedance of general voltage measuring instruments such as frequency response analyzer (FRA) and oscilloscopes is on the order of a few megaohm, making the voltage division caused by contact resistance negligible.

## IV. Measurement Results and Experimental Validation

This section verifies the validity of the proposed parasitic inductance measurement technique. First, measurements are performed on a commercially available MCPM shown in Fig. 4. Next, the measured values are analyzed. Finally, the validity of the measurement results is experimentally evaluated.

### *A. Experimental Results*

In this study, the measurement principle described in Fig. 3 was implemented using the measurement system shown in Fig. 13, which is based on a FRA. The measurement terminals are connected to the MCPM at the open ends created by cutting substrate trace, as shown in Fig. 10(a). Fig. 14(a) shows the measurement setup used to extract the parasitic inductances in the MCPM introduced in Fig. 4. This measurement setup follows Fig. 13 and procedure described in Chapter 3. Note that the current sensing shunt resistor

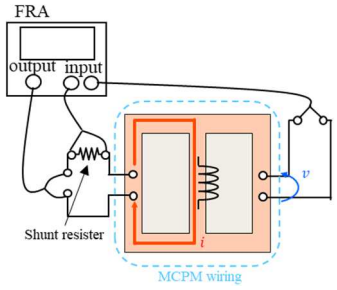
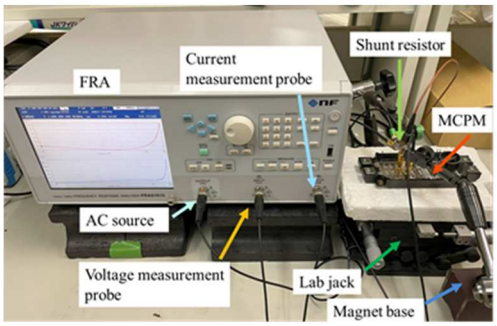



Fig. 13. Measurement system based on measurement principle shown in Fig. 3

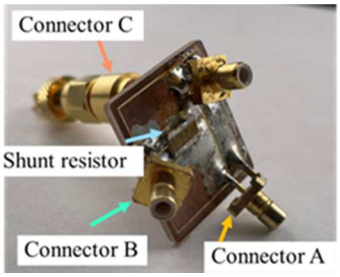
shown in Fig. 13 is not mounted on the MCPM itself, but instead implemented on a dedicated measurement board, as shown in Fig. 14(b). On this board, a shunt resistor is connected in series between Connector A and Connector C, and Connector B is connected across the shunt resistor terminals. By connecting Connector A to the output terminal of the FRA, Connector B to the current measurement input of the FRA, and Connector C to the MCPM, it is possible to measure the current flowing into the MCPM. Table 1 summarizes the measurement instruments and circuit components used in the setup, while Table 2 lists the measured parasitic inductances. The values shown in Table 2 correspond to the equivalent circuit model presented in Fig. 6.

### B. *Analysis of Negative CSI Values*

In Table 2, the values of $L_{cs1}$ to $L_{cs8}$ corresponding to CSI are all negative. This is due to the spatial relationship among the power-source wire bonds, kelvin-source wire bonds, and gate wire bonds in each device. Fig. 15 shows the top view layout of these wire bonds in the MCPM used in this study. As shown in Fig. 15, compared to kelvin-source wire, the gate wire bond is placed closer to the power-source. As a result, when current flows through the wire bond, the norm of the vector potential $\boldsymbol{A}$ induced along the gate wire bond becomes larger than that along the kelvin-source wire bond. According to (12), the induced voltage $v$ depends on the vector potential $\boldsymbol{A}$, and thus flows from kelvin-source to gate under this condition. Since this study defines the positive current direction as flowing from gate to kelvin-source, the measured values in Table 2 appear negative. However, this sign is purely a result of the coordinate definition and is not a serious problem.




(a) Photograph of measurement setup




(b) Shunt resistor external mounting board for current sensing

Fig. 14. Parasitic inductance measurement setup

TABLE 1. LIST OF EXPERIMENTAL INSTRUMENT AND CIRCUIT ELEMENT

| Instrument and circuit element | Model Number (Manufacturer) |
|---|---|
| FRA | FRA51615(NF) |
| Shunt resistor | Y16061R00000B9W(Vishay) |
| Silver paste | CN-7120(KAKEN TECH) |

$$v = -\int_{\text{Kelvin-Source}}^{\text{Gate}} \frac{\partial \boldsymbol{A}}{\partial t} \cdot d\boldsymbol{l} \tag{12}$$

### C. *Validation Experiment*

This section experimentally validates the measured parasitic inductances presented in the previous section. The validation involves confirming that the equivalent circuit model shown in Fig. 6, with the values from Table 2, reproduces the resonance behavior of the actual MCPM. As shown in Fig. 16, we define multiple closed loops of different sizes within the equivalent circuit model. For each loop, we compare the total parasitic inductance of the corresponding branches in the equivalent circuit model with the self-inductance of the loop measured using an impedance analyzer. To evaluate the accuracy of the proposed method, we vary the number of branches within each loop. This approach allows us to investigate how cumulative errors scale with the number of branches.

We determine the self-inductance using parallel resonance. Each closed loop defined in Fig. 16 is physically formed using silver paste, and a ceramic capacitor is inserted in series within the loop. We then connect the impedance analyzer probes across the capacitor and measure the impedance characteristics. From the resonance peak in the impedance spectrum, we extract the self-inductance. However, parasitic components in the wires and the capacitor itself shift the

TABLE 2. PARASITIC INDUCTANCE MEASUREMENT RESULT

| (nH) | | | | | | | |
|---|---|---|---|---|---|---|---|
| $L_{dd1}$ | 1.99 | $L_{g1}$ | 4.77 | $L_{kk1}$ | 5.66 | $L_{ss2}$ | 0.280 |
| $L_{dd2}$ | 1.93 | $L_{g2}$ | 5.17 | $L_{kk2}$ | 3.06 | $L_{ss3}$ | 0.265 |
| $L_{dd3}$ | 2.78 | $L_{g3}$ | 4.80 | $L_{kk3}$ | 6.54 | $L_{ss4}$ | 0.0143 |
| $L_{dd4}$ | 1.97 | $L_{g4}$ | 4.73 | $L_{kk4}$ | 2.24 | $L_{ss5}$ | 1.02 |
| $L_{dd5}$ | 2.40 | $L_{g5}$ | 4.91 | $L_{kk5}$ | 5.96 | $L_{ss6}$ | 0.334 |
| $L_{dd6}$ | 2.19 | $L_{g6}$ | 5.18 | $L_{kk6}$ | 2.02 | $L_{ss7}$ | 0.103 |
| $L_{dd7}$ | 1.32 | $L_{cs1}$ | -1.03 | $L_{kk7}$ | 4.36 | $L_{s1}$ | 4.99 |
| $L_{gg1}$ | 6.42 | $L_{cs2}$ | -0.716 | $L_{k1}$ | 2.68 | $L_{s2}$ | 5.81 |
| $L_{gg2}$ | 2.33 | $L_{cs3}$ | -1.45 | $L_{k2}$ | 3.01 | $L_{s3}$ | 5.31 |
| $L_{gg3}$ | 4.66 | $L_{cs4}$ | -1.06 | $L_{k3}$ | 3.44 | $L_{s4}$ | 5.93 |
| $L_{gg4}$ | 2.62 | $L_{cs5}$ | -1.16 | $L_{k4}$ | 3.15 | $L_{s5}$ | 5.02 |
| $L_{gg5}$ | 6.64 | $L_{cs6}$ | -0.772 | $L_{k5}$ | 2.83 | $L_{s6}$ | 5.10 |
| $L_{gg6}$ | 1.13 | $L_{cs7}$ | -0.661 | $L_{k6}$ | 3.46 | $L_{s7}$ | 4.07 |
| $L_{gg7}$ | 3.47 | $L_{cs8}$ | -0.552 | $L_{ss1}$ | 6.02 | | |

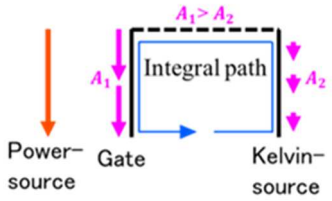



Fig. 15. Image of wire bond position from above

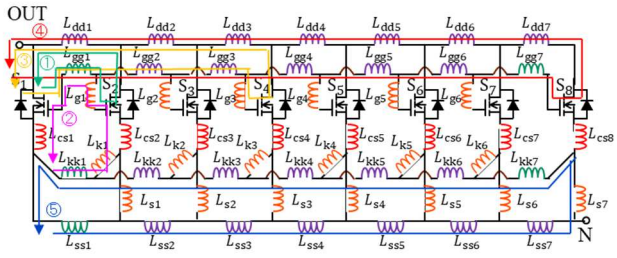



Fig. 16. Closed loop definition for validation experiment

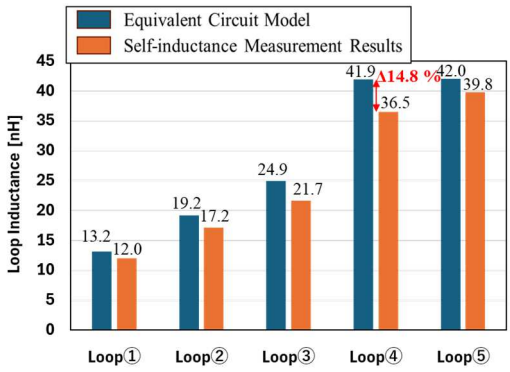



Fig. 17. Validation experiment result

resonance point. To account for this, we fit the impedance response of an extended equivalent circuit including parasitic to the measured data, allowing accurate estimation of the loop's self-inductance.

Fig. 17 compares the modeled parasitic inductance with the measured self-inductance for each loop in Fig. 16. The resulting error rates range from 5.53% to 14.8%, indicating that the equivalent circuit can replicate the MCPM's internal resonance behavior with about 2.66% to 6.67% accuracy in resonance frequency. Considering the typical manufacturing tolerances of the parasitic capacitances in SiC MOSFETs, this accuracy is acceptable. For instance, reference [14] reports that even devices from the same batch exhibit significant capacitance variation, with gate-to-source capacitance showing deviations of approximately ±10% across 30 devices. Given this, actual tolerances may be even larger. Therefore, the main reason for the resonance frequency deviation in the developed equivalent circuit model is the tolerance of parasitic capacitances.

## V. Conclusion

This paper proposed a measurement-based method for extracting parasitic inductance in MCPMs. The proposed approach addresses the limitations of conventional methods, particularly their applicability to complex structures and feasibility for experimental measurement. We applied the method to a commercially available MCPM with an eight-parallel half-bridge structure and performed inductance measurements. The validity of the measured parasitic inductance was experimentally verified. The results confirmed that the measurements were accurate and demonstrated that the proposed method enables systematic extraction of parasitic inductance in MCPMs based on actual measurements.

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