Non-isolated Interleaved High Step-down DC-DC Converter with Reduced Switched Capacitor Stages for Data Center Applications

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***Abstract*— In recent years, the power supply system for data centers requires high efficiency, high power density converters with high step-down ratios for power conversion from 48 V to loads requiring low voltage and high current. The previous study proposed a non-isolated switched capacitor (SC) converter with a high voltage step-down ratio and a more compact design. This converter reduces the number of stages of the SC compared to conventional topologies. The converter has been tested at low output currents, but not at high currents. In addition, the use of isolated power supplies in the gate drive circuit has led to a large-scale circuit board. In this paper, a prototype circuit was developed for high-current applications and its operation was verified. As a result, the converter successfully operated up to 90A, achieving a power density of 18.22 W/in³. This demonstrated the potential of the proposed converter as a high-power-density PoL converter.**

Keywords—dc-dc converter, high step-down converter, Switched capacitor, high-power density, gate drive

I. INTRODUCTION

In recent years, with the global development of the information society, the increasing power consumption in data centers has become a significant issue [1, 2]. As a result, data centers require power supply systems that are highly efficient and have high power density. A promising power supply system that meets these demands is the high-voltage direct current (HVDC) system.

Figure 1 illustrates the conventional AC power supply system and the HVDC system. In the AC power supply system, power is distributed from an uninterruptible power supply (UPS) to servers at AC 100–200V. The emergency battery within the UPS operates on DC, while the CPUs and memory within the servers operate at DC 5V, 3.3V, and 1V. Therefore, as shown in Figure 1, the AC power supply system requires a total of four power conversion stages, resulting in significant power conversion losses.

On the other hand, in an HVDC system, high-voltage DC power is directly supplied to the servers. This eliminates unnecessary AC-DC and DC-AC conversion stages, thereby reducing installation space and improving efficiency. Furthermore, the use of high-voltage power lines allows for thinner wiring, which also contributes to reducing installation space.

However, despite these advantages, the HVDC system requires high-performance step-down converters, known as point-of-load (PoL) converters, to supply stable DC power to internal server components such as CPUs.

In modern data centers, PoL converters are required to step down a 48V DC bus to a low voltage (around 1V) and supply high current (100A) to the load. However, conventional PoL converters commonly used in data centers, such as buck converters, do not have a sufficient step-down ratio and require multiple step-down converters connected in series to achieve the desired voltage reduction. As a result, the current delivery path is becoming longer, hindering system miniaturization and reducing overall efficiency.

To address this issue, various high step-down ratio converter topologies have been proposed. These converters include transformer-based converters [3]-[6] and switched capacitor (SC) converters [7]-[9]. Transformer-based converters generally use ferrite cores in their transformers, but ferrite is not well-suited for frequencies above 1 MHz, which hinders miniaturization through high-frequency operation.

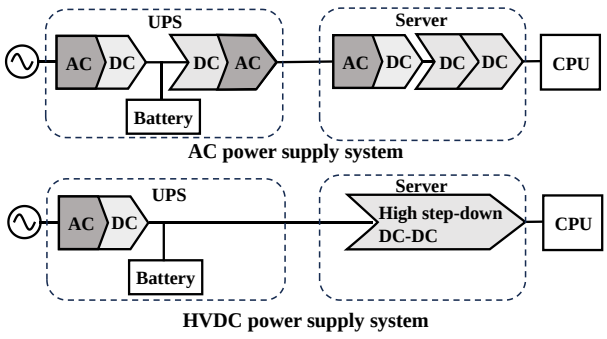


Fig.1. Power supply system for data centers

On the other hand, SC converters do not use transformers, allowing for high-frequency operation. However, SC

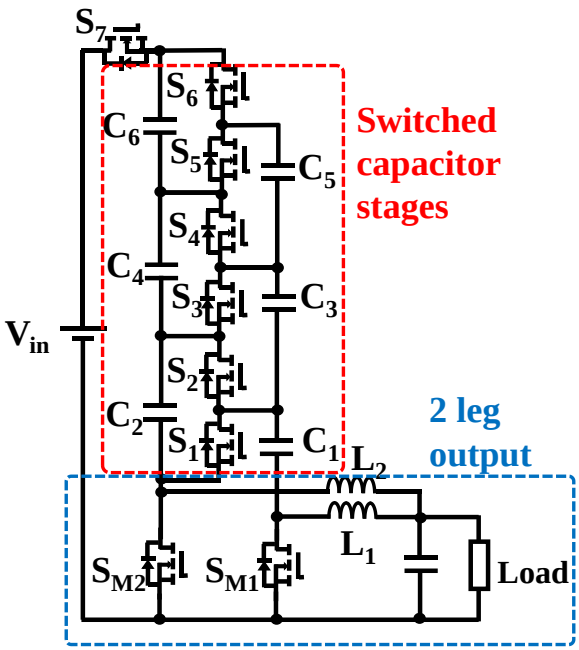


Fig.2. Non-isolated High Step-down DC-DC Converter with Reduced Switched Capacitor Stages and Automatic Current Sharing

converters require multiple SC stages to achieve a high step-down ratio, which increases the number of components. As a result, achieving high power density becomes difficult.

To solve this problem, a previous study proposed an SC converter [10] that achieves a high step-down ratio with fewer SC stages compared to conventional SC converters. However, prior research has only conducted experiments to verify the operating principle, and performance evaluation under high-current conditions for practical applications has not been carried out. Furthermore, the gate drive circuit used an isolated power supply, leading to an increase in circuit board size.

In this paper, a cascaded bootstrap circuit is applied to the gate drive circuit to achieve a compact circuit board, and a prototype circuit suitable for high-current applications is developed. The performance is then evaluated under high-current conditions assuming practical applications, and potential issues under high-current operation are identified.

II. Review of the Previous Studies on SC Converter

A. Circuit Topology

Figure 2 shows the SC converter proposed in previous research. The converter shown in Figure 1 consists of an SC stage that steps down the infiput voltage to 1/7 and two series capacitor converter stages that perform step-down conversion through duty cycle control. This converter improves the step-down performance by forming an interleaved output through the addition of SM1, SM2, L1, L2, and C1 to the previously proposed converter [11], as discussed later.

Additionally, this converter achieves interleaved operation by operating switches Sa and Sb with a 180-degree phase shift. Switches S1, S3, ... operate complementarily to SM2, while switches S2, S4, ... operate complementarily to SM1. This converter does not allow a moment when both SM1 and SM2 are off-state. If the duty cycle of SM1 and SM2 is less than 0.5, a shoot-through current may flow in the SC stage (e.g., the current loop of S1, S2, and C2). Therefore, the duty cycle of SM1 and SM2 must be greater than 0.5. The detailed operating principles are described in [10].

B. Characterisics of the previous studies on sc converter

The converter shown in Fig. 2 consists of an SC stage and a series capacitor converter stage that performs step-down conversion by controlling the duty cycle. As stated in [12], the duty cycle of the high-side switch in the series capacitor converter is twice that of a conventional buck converter. As a result, the converter in Fig.2 can achieve the same step-down ratio as the converter in [11] with only half the number of SC stages.

Additionally, the converter in Figure 1 has advantageous features for miniaturization. Since each component experiences lower voltage stress, smaller components can be used. Furthermore, the output stage is equipped with an interleaved output, which reduces output current ripple. This contributes to reducing the total size of the inductors required for output current smoothing.

However, in conventional converters with interleaved outputs [13]–[15], special control is required to balance the currents of the two output inductors. This increases the size of the controller circuit due to the need for current sensing and feedback control. In contrast, this converter can automatically balance the inductor currents without additional control, enabling the implementation of a simpler controller.

III. Miniaturization Of Gate Driver Circuits

In previous research, the SC converter proposed in [10] used an isolated power supply for gate driving to verify its operating principles, resulting in a significantly large circuit board. Considering its application in data centers, this large board size hinders both implementation in limited installation space and improvements in cooling efficiency. Therefore, this paper achieves circuit board miniaturization by applying a cascaded bootstrap circuit to the gate drive circuit.

The cascaded bootstrap circuit [16] is an extension of the widely used bootstrap circuit, which is commonly employed for driving the high-side switch of a buck converter. It has been frequently applied in converters such as flying capacitor multilevel (FCML) converters, which contain multiple floating switches. The cascaded bootstrap circuit is particularly advantageous because, unlike isolated power supplies, it can be implemented using compact ceramic capacitors and diodes, making it highly effective in reducing circuit board size.

However, in a multi-stage configuration, the higher stages suffer from the forward voltage drop of the diodes, which may prevent the circuit from supplying sufficient gate voltage to properly drive the switches. Therefore, ensuring that the upper-stage gate voltage remains sufficient is a crucial design consideration.

A. Cascaded Bootstrap Circuit on Previous Studies SC Converter

Figure 3 shows the circuit diagram of [10] with the cascaded bootstrap circuit applied. The cascaded bootstrap circuit in Fig.3 consists of bootstrap capacitors

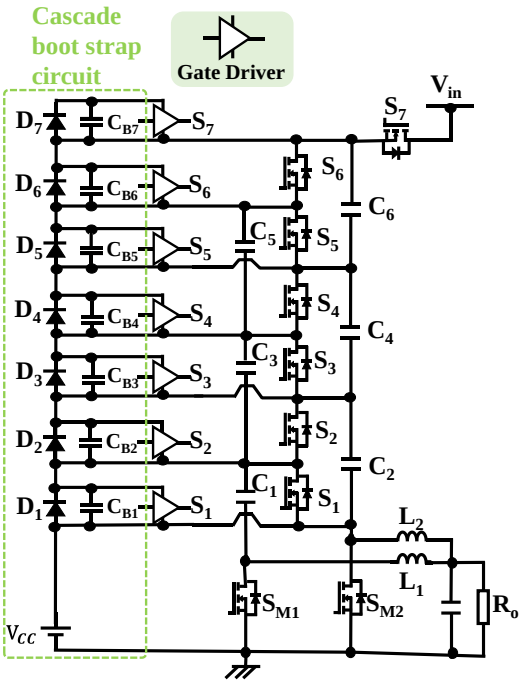


Fig.3 A non-isolated high step-down converter with an applied cascade bootstrap circuit

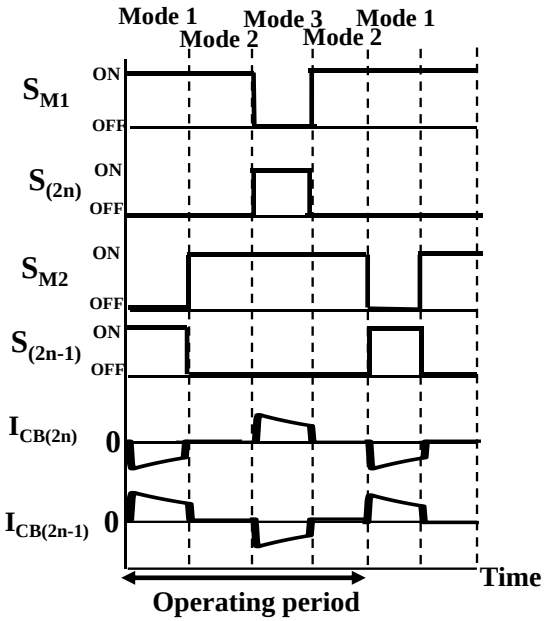


Fig.4. Switching patterns and current waveforms of the bootstrap capacitor

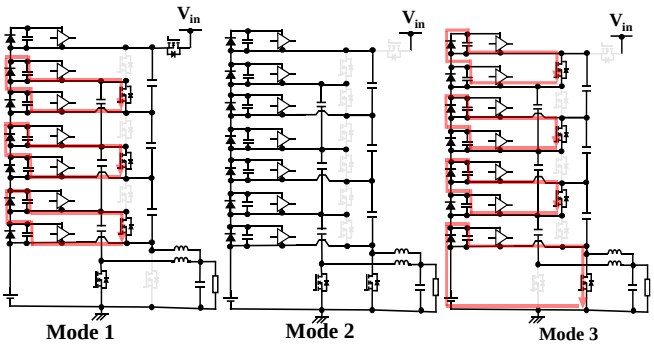


Fig.5. Current patterns of the cascade bootstrap circuit

C_{B1}~$C_{B7}$and bootstrap diodes D_1~D_7, which are connected to gate drivers that supply gate voltage to MOSFET S_1~S_7.

In the converter presented in [11], stepping down 48V to 1V requires six SC stages (assuming extreme duty cycles are avoided to maintain efficiency). When applying the cascaded bootstrap circuit, the upper-stage switches cannot receive sufficient gate voltage. However, in the converter shown in Figure 3, the number of required SC stages is reduced by half, enabling the cascaded bootstrap circuit to supply sufficient gate voltage even to the topmost switch.

As a result, the gate drive circuit can be miniaturized without using an isolated power supply, significantly reducing the overall circuit board size.

B. Operating Principles of the Cascade Bootstrap Circuit

Figure 4 shows the switching pattern and the current waveform of the bootstrap capacitor, while Figure 5 illustrates the current pattern of the bootstrap circuit in each mode. The bootstrap capacitor C_{B1} is charged from V_{cc} through D_1 and SM2 during Mode 3. Similarly, C_{B2} is charged from C_{B1} through D_2 and S_1 during Mode 1. In the same manner, the other bootstrap capacitors are charged from the bootstrap capacitor of the lower stage

IV. Thermal Design of the PCB

When operating the circuit in Fig. 3 under high-current conditions, particularly large currents flow through the current path around the inductor and the path carrying the output current. Additionally, in the SC stage, the lower-stage capacitors bear a greater current load, which is expected to cause significant heating due to ripple current during charging and discharging. Therefore, it is crucial to design a PCB that is both compact and capable of providing sufficient heat dissipation performance.

A. Paths of Output Current and Inductor Current

Generally, when manufacturing circuit boards, the copper foil on a PCB with a thickness of 35 μm is designed with a guideline of allowing a current of 1A per 1mm trace width to keep the temperature rise within 10°C. For high-current applications, heat dissipation performance is typically improved by increasing the copper foil thickness or using a metal-based heat dissipation substrate. However, due to the complexity of the wiring patterns in this design, a four-layer PCB was adopted, and the maximum manufacturable copper thickness was limited to 70 μm. To further enhance heat dissipation, the solder resist covering the copper foil was removed, and additional copper plates were soldered on top to increase the thickness.

B. Current Path of the Switched Capacitor

The current flowing through the switched capacitors increases toward the lower stages of the SC stage, with C1 and C2 carrying three times the current of C5 and C6, and C3 and C4 carrying twice the current. Therefore, when implementing the circuit on the PCB, the number of capacitors connected in parallel for C5 and C6 was determined based on their ripple current heating characteristics. To address heat dissipation, C1 and C2 were implemented with three times the number of parallel capacitors as C5 and C6, while C3 and C4 were implemented with twice the number.

TABLE I. TABLE TYPE STYLES

Input Voltage V_{in}	48 V
Control power supply voltage V_{cc}	11 V
Operating frequency	500 kHz
Load R_o	Constant Current Load (TAKASAGO FK-1000L2)
Inductors L1, L2	120 nH, 0.145 mΩ DCR (EATON FP1010R-R120-R)
Capacitors C_1~C_6	10uF (Murata GCM31CD71H106KE35)
MOSFET S_1~S_7	BSZ063N04LS6ATMA1
MOSFET S_{M1}, S_{M2}	IQE006NE2LM5ATMA1
Bootstrap capacitor C_{B1}~C_{B7}	10uF (Murata ZRB18AR61E106ME01L)
Bootstrap diode D_1~D_7	PMEG4005EPK,315

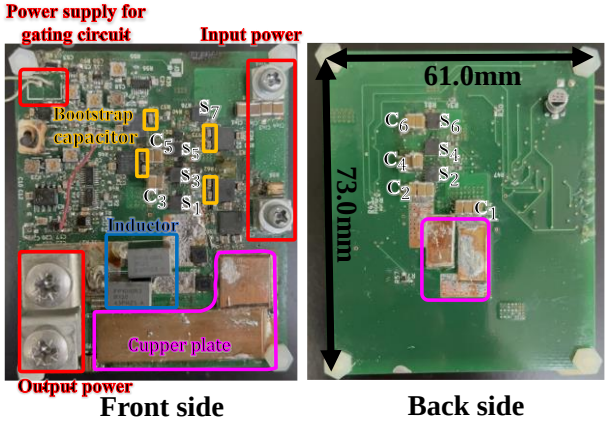


Fig.6. Photo of the prototype of the high step-down converter for application implementation

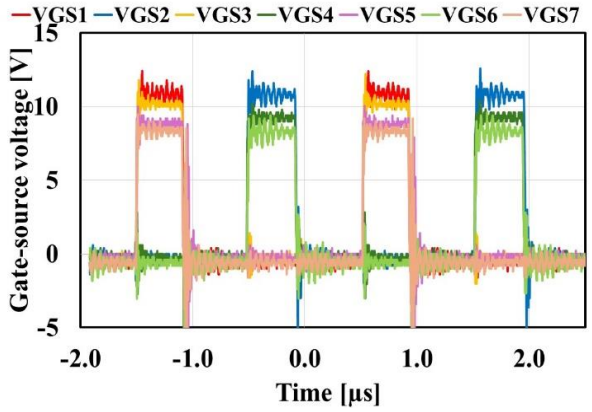


Fig.7. Gate-source voltages of S1 to S7

V. EXPERIMENT

An experiment was conducted to verify the operation of the cascaded bootstrap circuit and evaluate its performance under high-current conditions in the converter shown in Fig. 3. The prototype converter was designed with three switched-capacitor stages, as illustrated in Fig. 3.

Table I presents the specifications of the prototype, and Figure 6 shows a photograph of the prototype. In this experiment, a low switching frequency of 500 kHz was selected to facilitate the observation of voltage waveforms under high-current conditions using an oscilloscope.

A. Gate-to-source voltage waveform

Figure 7 shows the gate-source voltages of S1 to S7. In the experimental waveforms, VGS decreases as it moves to the upper stages due to the influence of the diode's forward voltage, however, sufficient voltage is supplied to operate the switches. Although switching noise was visible in the measured VGS waveform, the VGS itself was confirmed to operate as theoretically possible even during high-current operation.

B. Output Voltage

Figure 8 shows the relationship between the output current and output voltage (theoretical and measured values when the duty cycle is fixed at 0.71). Additionally, Factor 1 and Factor 2 in Figure 6 indicate the proportion of the causes of output voltage drop. Figure 9 shows the waveforms of the gate-to-source voltage (measured) and the drain-to-source voltage (measured and lossless simulation) of SM1 during the transition from Mode 2 to Mode 3 when the output current is 70A. As shown in Figure 6, the output voltage decreases as the output current increases.

The primary causes of this voltage drop can be attributed to two factors. The first factor, as indicated by Factor 1 in Fig.9 , is that the drain-to-source voltage of SM1 in its off-state is 6.8V in the simulation, whereas the measured waveform shows approximately 5.8V, which also applies to SM2. As a result, the voltage applied to the inductor becomes lower than expected, leading to a reduction in the output voltage. This phenomenon is caused by the losses occurring in the SC stage. The second factor, as indicated by Factor 2 in Fig.9 , is that the actual duration of the drain-to-source voltage is shorter than that in the ideal simulation. This is due to the minority carrier storage effect in the MOSFET, which causes the effective duty cycle to be longer than the set value during high-current operation. This issue can be mitigated by using MOSFETs with superior reverse recovery characteristics.

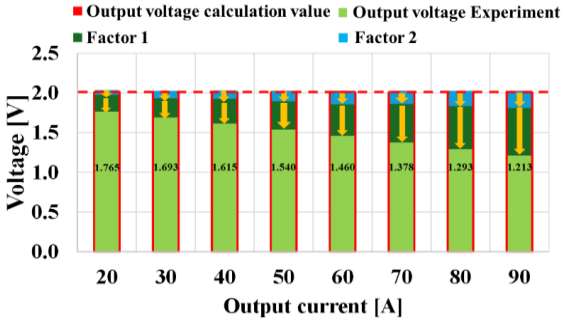


Fig. 8. Relationship output voltage against output current, as well as the rate of output voltage drops, when the duty cycle is fixed at 0.71.

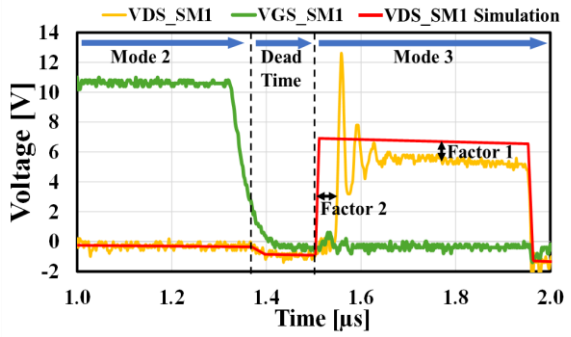


Fig. 9. The waveforms of the gate-to-source voltage and drain-to-source voltage of SM1 during the transition from Mode 2 to Mode 3.

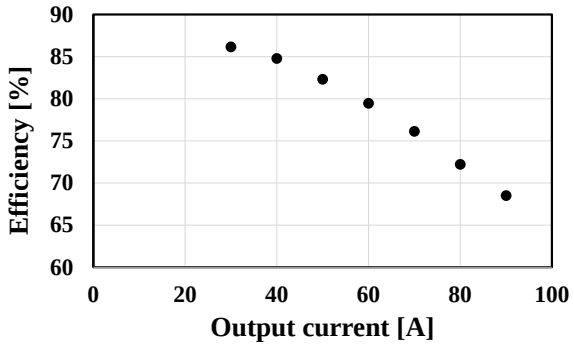


Fig.10. Measured efficiency at duty cycle 0.71

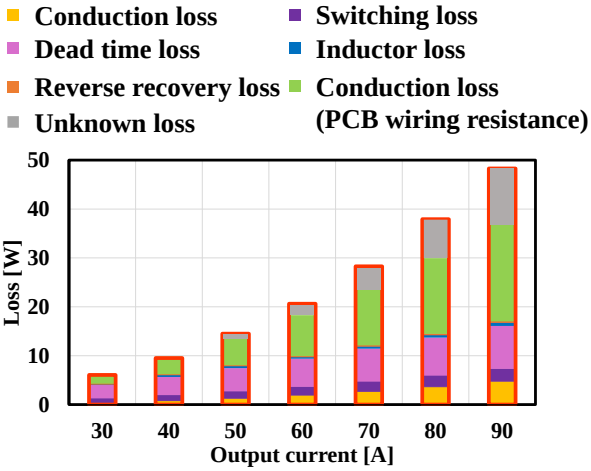


Fig.11. Loss analysis results

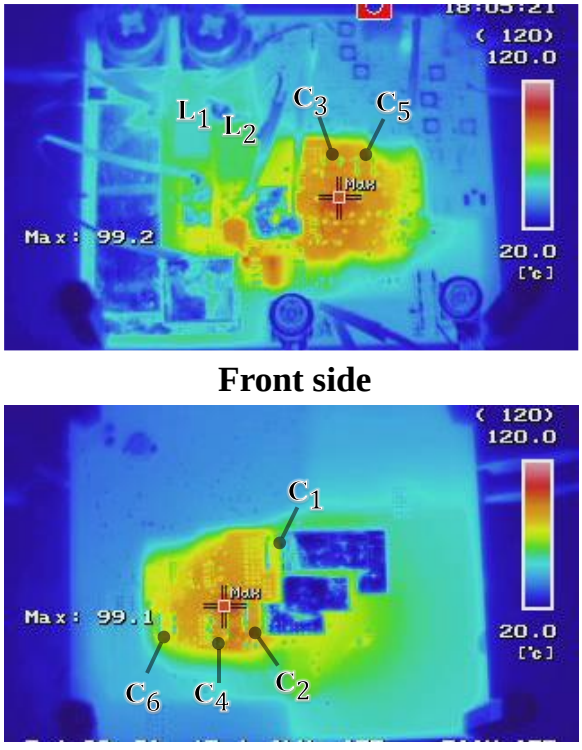


Fig.12. Temperature distribution captured by the thermal camera during the experiment at an output current of 40A.

C. *Efficiency and loss analysis*

The efficiency was evaluated by fixing the duty cycle at 0.71 and varying the output current from 30A to 90A using a constant current load. The results are shown in Figure 10. From Fig.10, it can be observed that the efficiency decreases as the output current increases. Additionally, Figure 11 presents the results of the loss analysis. The analysis revealed that the primary contributors to the losses were the losses occurring during dead time due to current flowing through the body diode and the conduction losses caused by the wiring resistance on the PCB. Regarding the losses during dead time, it is expected that they can be reduced by implementing Adaptive Dead Time Control. Furthermore, to address the conduction losses due to PCB wiring resistance, a thermal analysis will be conducted to identify the specific areas where these losses occur, and improvement methods will be discussed.

D. *Thermal analysis*

Figure 12 shows a thermal image captured using an infrared camera. This image was taken under a condition where the output current was 40A without fan cooling. From Fig12, it was confirmed that the temperature rise of the copper plates installed around the output side and the inductor, where a particularly large current flows, was suppressed to approximately 20°C. Additionally, the temperature rise of the switched capacitors in the SC stage was effectively controlled by implementing an appropriate number of parallel capacitors.

However, it was observed that switches S3 and S4 in the SC stage experienced significant heating, causing an increase in the temperature of surrounding components. The reason for this is considered to be the insufficient heat dissipation area of S3 and S4. While S1, S2, S5, and S6 had sufficient heat dissipation area, S3 and S4 were placed in close proximity to each other due to miniaturization constraints, preventing adequate heat dissipation.

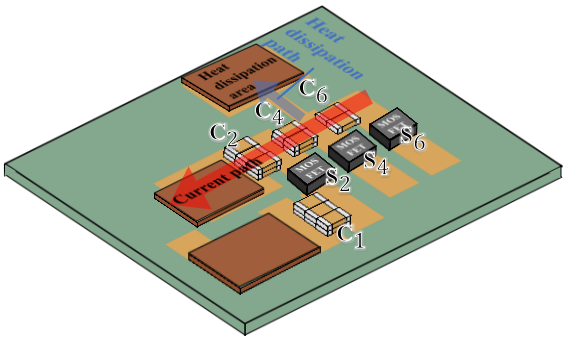
Furthermore, the PCB was designed so that current flows between the top and bottom layers through vias. However, to secure a sufficient heat dissipation area, the current path became longer, increasing wiring resistance and leading to higher losses.

As a solution to this issue, as shown in Figure 13, the current path of the SC stage can be shortened, and heat dissipation paths can be extended from the current path to the unoccupied areas of the PCB to increase the heat dissipation area.

VI. Conclusions

In this paper, we miniaturized the gate drive circuit of a non-isolated high step-down DC-DC converter with interleaved output, which was proposed in previous research with a reduced number of SC stages and evaluated the circuit board under high-current conditions for application feasibility. As a result, by applying a cascaded bootstrap circuit, we successfully reduced the PCB size while confirming that the circuit operates as theoretically expected even under high-current conditions. Additionally, it was revealed that under high-current conditions, the output voltage of this converter decreases more than expected due to the minority carrier storage effect in the MOSFETs of the series capacitor

converter stage. Furthermore, it was found that dead-time losses and losses due to wiring resistance in the SC stage account for a significant portion of the total losses. These issues can be improved by adopting MOSFETs with superior reverse recovery characteristics, implementing appropriate dead-time control, and designing the PCB to shorten wiring while ensuring sufficient heat dissipation area.



Back side of PCB

Fig.13 Thermal design in the SC stage

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