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***Abstract*— Recently, as the miniaturization and densification of the power conversion circuit, switching frequency has been increased. To accomplish the densification, it is essential to predict the losses that occur in each part for the optimization of electric components. However, switching loss which needs to consider nonlinear characteristics are difficult to predict. As a solution, considering the dependence of the gate-drain capacitance on gate-source voltage may improve the prediction accuracy of switching loss. The purpose of this study is to evaluate the improvement of prediction accuracy by considering it. First, to construct the simulation model, the wiring parameter in the circuit, static characteristics and the parasitic capacitance of the device was measured. Next, the device model provided by the manufacturer to use in the simulation was adjusted. Also, the characteristics of the gate-drain capacitance on the gate-source voltage were obtained from two types of measurement circuits. As a result, it was verified that the difference which occurred at the rise of the drain-source voltage at the turn-off tended to decrease and prediction accuracy of the turn-off loss was improved by considering the characteristics of the gate-drain capacitance on the gate-source voltage. Therefore, we concluded that this consideration has the ability to the improvement of turn-off waveforms.**

Keywords— switching; Spice simulation; gate-drain capacitance; wiring parameter; parasitic inductance

I. INTRODUCTION

Power conversion circuits are used in many applications, such as machinery and tools, electric vehicle (EV) [1], home appliances, digital equipment. In particular, switching devices included in power conversion circuits have mainly used Si-MOSFET. However, its performance is getting to the limit [2]. Therefore, SiC-MOSFET and GaN-FET, known as high speed switching devices have been used as the next-generation switching devices [3-5].

This attractive feature helps that power conversion circuit can be miniaturization and densification Because of the miniaturization and the densification, to reduce the size of the components is also necessary. However, to achieve sufficient heat dissipation, we need to attach a bulky heat sink, which prevents miniaturization of components. Also, high switching frequency reduces the size of the magnetic components. However, as the switching frequency is high, heat dissipation performance is low. Hence, switching frequency and heat dissipation design performance is a trade-off relationship. Therefore, to make optimal heat dissipation design, device losses must be correctly predicted.

However, the measurement of switching waveform is becoming difficult for recent high speed switching loss devices. There are mainly three reasons. First is the frequency limit of probes. Second is the installation space of probes. Third is the signal delay of probes. For these reasons, the measurement of next-generation devices is almost impossible. Therefore, switching loss estimation by simulation is an important design tool for recent high speed switching devices.

However, there are two main problems to solve, especially in fast switching. the first problem is that there is a deviation from the device model and the actual device. The second problem is the modeling of PCB.

To solve the first problem, many studies have been reported that modeled switching device and verified prediction accuracy of switching characteristics [6-11]. According to [6], a simulation model was constructed based on information of the datasheet, and switching waveforms were compared. However, there was a deviation in the mirror period and a deviation occurs at the rise of drain-source voltage v_{ds} waveform (Fig.9 conventional). In this period, gate-source voltage v_{gs} is not 0V. Also, gate current flows through C_{gd} and it is charged and discharged. Here, the datasheet shows the parasitic capacitance when v_{gs} is 0V, but only a part of the actual power conversion circuit can be covered. Therefore, it was suggested that further modeling of C_{gd} was necessary. On the other hand, the v_{gs} characteristics of C_{gd} was modeled in [10]. It was reported that this modeling further improved prediction accuracy. However, the characteristic of C_{gd} was extracted by back calculating the switching waveform with a long mirror period. Although the modeling of the MOSFET, which was their purpose, was achieved, it does not follow our purpose of predicting the switching waveform.

Next, in PCB modeling at high speed switching, the voltage drop of the wiring parameter, especially parasitic inductance, is a significant problem [12-14]. Conventionally, the estimated value of inductance was obtained by fitting from the measured

switching waveform. However, the value of inductance is approximately a few nanohenries order and it is not practical because accurate measurement becomes increasingly difficult. To solve this problem, previous research [15,16] proposed a common source inductance (L_s) measurement method that was particularly difficult to measure in the state of being mounted on PCB and enabled to measure it. Therefore, the modeling of PCB could be done without using estimate value.

The purpose of this paper is to verify the improvement of prediction accuracy by considering the dependence of C_{gd} on v_{gs} in the model. In order to evaluate the prediction accuracy of the switching waveforms, we measured the wiring parameter in the PCB, the parasitic capacitance, and the static characteristics of the MOSFET. In this paper, we adopted the double pulse test (DPT). Also, in order to verify the accuracy of the predictions with and without consideration of the dependence of C_{gd} on v_{gs}.

The following discussion consists of 4 sections. Section II explains the construction method of the conventional model. Next, section III explains the construction method of the proposed model. Then, in section IV, the experimental result and each model are compared. Finally, section V gives the conclusions.

II. Conventional Model

This section explains the conventional model. Firstly, the static characteristics and the characteristics of the parasitic capacitance to the drain-source voltage V_{ds} of the devices shown in Table I were measured by curve tracer. Also, the parasitic inductances in the circuit (L_d, L_g, and L_s) were measured by method in [17], and parasitic resistance of main circuit loop R_d was measured by impedance analyzer.

A. Modeling of PCB

In this subsection, we measured the wiring parameter in the PCB. Also, the wiring parameter is a constant value, so measurement is very important. In order to measure the wiring parameter, we used three types of circuits.

Measurement of L_s was adopted a recently proposed method [15,16]. The measurement circuit is shown in Fig.1(a). First, another PCB with the same pattern as the experimental circuit prepared and low-side MOSFET mounted. Next, a resistor R_{mesu} with high impedance was mounted on the position of the gate resistance R_g. Also, a ceramic capacitor C_{mesu} with much larger of the gate-source capacitance in MOSFET was mounted to connect the pads for the output terminal and the ground terminal of the gate driver. In addition, we made the solder bridges to connect the pad for high-side parasitic diode. Then we applied the DC voltage to C_{mesu} in order to keep the MOSFET at the on-state. Finally, we connected a signal generator between the drain and source of MOSFET to supply the high-frequency sinusoidal current and measured the AC voltage across R_{mesu} and AC current from the signal generator. The RMS of v_{ds} and v_{gs} are defined as V_{mesu} and I_{ac}, respectively.

In the high-frequency region, C_{mesu}, C_{iss}, and L_g can regard as short because its impedance is far lower than R_{mesu}. Therefore, v_{mesu}, the voltage drops at R_{mesu} and L_s are approximately the same. Consequently, the value of L_s can be calculated as

TABLE I. Model Number of Measured Devices

S_1	Model number (Manufacturer)	Package
A	IRFR4620PBF (Infineon)	DPAK
B	IRFB5620PBF (Infineon)	TO-220
C	FDPF770N15A (ON Semiconductor)	TO-220
D	FDMC86240 (ON Semiconductor)	MLP

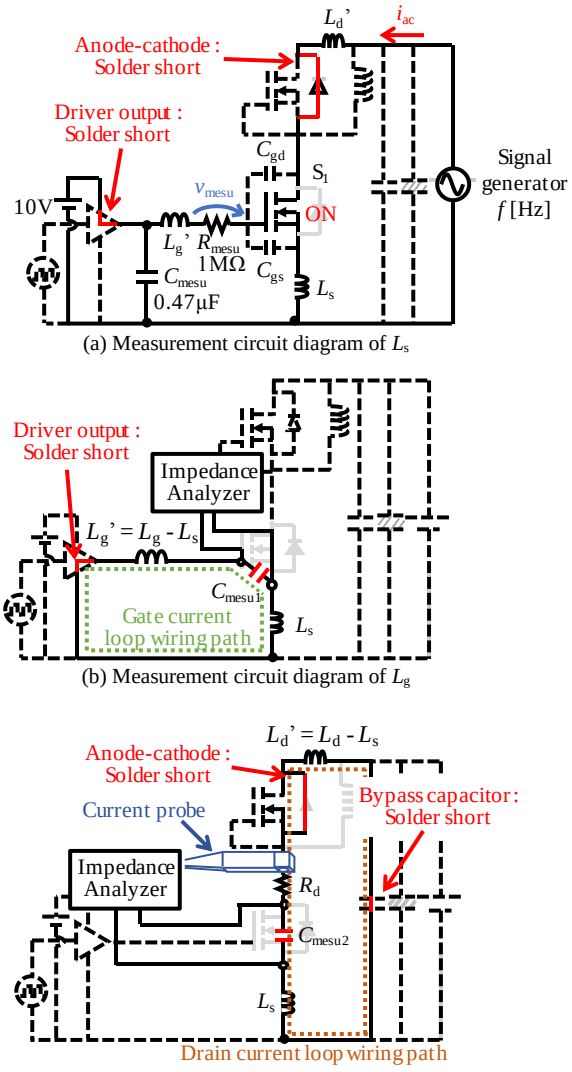


Fig.1. Circuit diagram of measurement for PCB modeling

$$L_s = \frac{V_{mesu}}{2\pi f I_{ac}} \sin\phi \,, \tag{1}$$

where f is the frequency of AC current and ϕ is the phase difference between the voltage drop at R_{mesu} and the AC current i_{ac}.

In this paper, we measured at nine AC frequency from 2MHz to 10MHz. Also, this measurement was carried out 2 times in each MOSFET. Then, we averaged the results to determine L_s.

TABLE II. THE LIST OF MEASURED WIRING PARAMETER

S_1	L_g' [nH]	L_d' [nH]	L_s [nH]	R_d [Ω]
A	7.97	25.99	2.38	1.06
B	3.66	26.70	4.67	0.925
C	4.36	46.30	5.46	1.46
D	5.40	29.04	1.17	0.71

Next, according to the method of literature [17], the parasitic inductance L_g and L_d were measured by impedance analyzer (IM7581 Hioki E.E. Corp.) using the parallel LC resonant between parasitic inductance and capacitor of known capacity. In addition, parasitic resistor R_d was also measured using an impedance analyzer. In each measurement, we prepared another PCB with the same pattern as the experimental circuit similarly to the measurement of L_s.

Firstly, the measurement circuit diagram of L_g is shown in Fig. 1(b). A small ceramic capacitor C_{mesu1} was mounted on the pads for gate and source terminal of S_1. In addition, we made a solder bridge between the pad for driver output and ground terminal. Finally, both ends of C_{mesu1} connected impedance analyzer. As a result, a parallel-connected LC resonator was composed of parasitic inductance L_g+L_s and the ceramic capacitor C_{mesu1} in the gate current loop wiring path.

Then, we measured the frequency dependency of capacitor C_{mesu1}. When the resonant frequency at the peak impedance is defined as f_{rg}, L_g' can be obtained as

$$L_g' = \frac{1}{4\pi^2 f_{rg}^2 C_{mesu1}} - L_s . \quad (2)$$

Next, the measurement circuit diagram of L_d is shown in Fig. 1(c). We mounted a small ceramic capacitor C_{mesu2} on the pads for drain and source terminals. Also, we made a solder bridge the pads for both ends of C_{mesu2}. In addition, we made a solder bridge between anode and cathode terminal of high-side parasitic diode. Moreover, to consider the parasitic inductance included in the current probe, a current probe inserted. Finally, both ends of C_{mesu1} connected impedance analyzer. As a result, a parallel-connected LC resonator was composed of parasitic inductance L_d+L_s and the ceramic capacitor C_{mesu2} in drain current loop wiring path.

Then, we measured the frequency dependency of capacitor C_{mesu2}. When the resonant frequency at the peak impedance is defined as f_{rd}, L_d' can be obtained as

$$L_g' = \frac{1}{4\pi^2 f_{rd}^2 C_{mesu2}} - L_s . \quad (3)$$

At last, the measurement of R_d was taken with the circuit from which C_{mesu2} was removed in Fig.1(c). and measured the frequency dependency of the resistance component. We determined the resistance value at resonant frequency f_{rd} as R_d. The measurement results are shown in Table II.

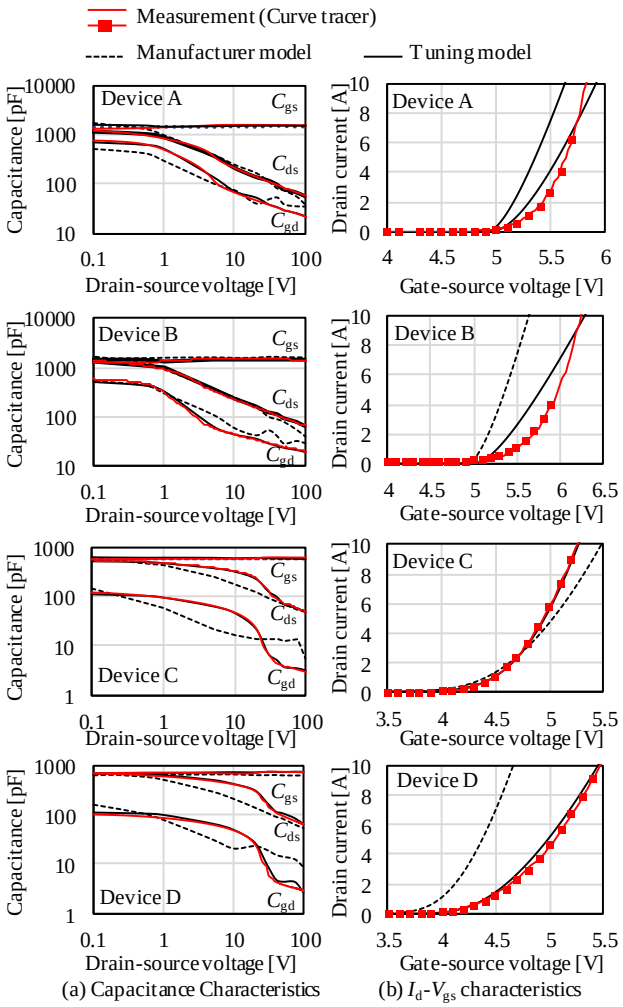


Fig.2. Comparison of measurement and model.

B. *Modeling of device*

In this subsection, we model the switching device so that the characteristics can fit the measurement data. In order to achieve this purpose, we used the device model provided by the manufacturer and the characteristics were adjusted to its measurement data.

The experimental value of parasitic capacitance and I_d-V_{gs} characteristics were measured by curve tracers CS-3300 and CS-605 (IWATSU ELECTRIC CO., LTD.), respectively. Parasitic capacitance was measured for v_{ds} of 0 to 100V and frequency of 1MHz. Also, I_d-V_{gs} characteristics were measured for I_d of 0 to approximately 10A. These measurements were performed on three different elements of the same model number. We averaged the acquired values and this was made into the measurement value.

Here, we modeled the device in PSpice. First, the parasitic capacitance included in the device model adjusted to be as negligible as possible. C_{ds} and C_{gd} with the dependence of V_{ds} were modeled using external voltage-controlled current sources GVALUE. The product of the capacity table and the time derivative of V_{ds} is described for these current sources. C_{gs}

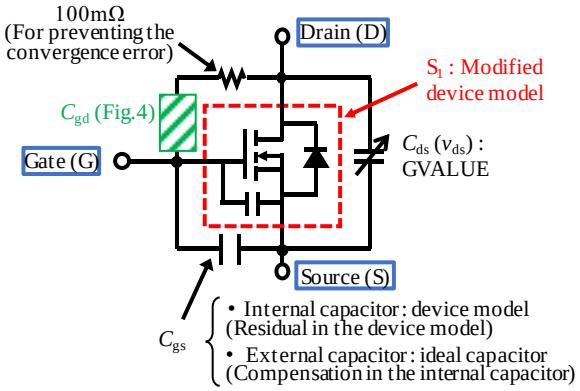


Fig.3. Modeling circuit of MOSFET constructed with PSpice.

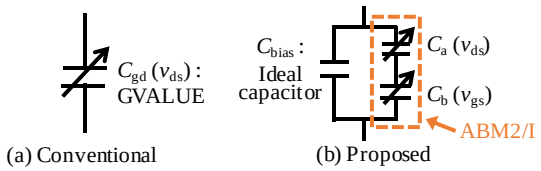


Fig.4. Modeling circuit diagram of C_{gd}

without the dependency of V_{ds} was modeled by an ideal capacitor except for the remaining capacity in the device model.

Next, we focused on the fact that the I_d can be changed by the ratio of the channel width W to the channel length L, these parameters in the device models were adjusted. The modeling result is shown in Fig.2. Manufacturer model is a device model provided by the manufacturer, and the tuning model is a device model that was tuned according to the method in this subsection. As shown in the Fig.2, we were able to model more accurate than the device model provided by the manufacturer.

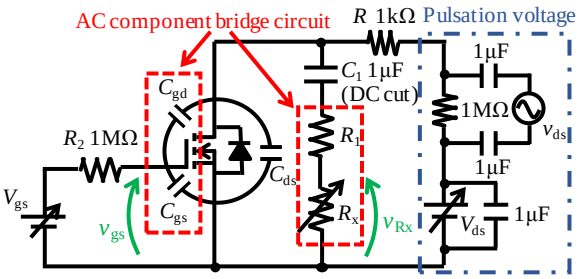
Also, Fig.3 shows the configured MOSFET model in PSpice. Moreover, Fig.4(a) shows the modeling circuit diagram of C_{gd} in the conventional model. In addition, to avoid convergence errors, we inserted a 100mΩ resistor in series with C_{gd} that does not affect the waveform.

III. Proposed Model

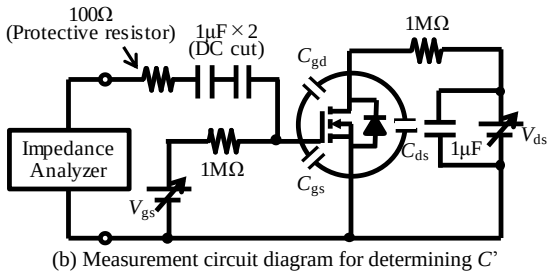
The proposed model added the dependence of V_{gs} on C_{gd} from the conventional model and described two variables function of V_{ds} and V_{gs}. Also, to extract its characteristics, two kinds of measurement circuits shown in Fig.5 were used.

The first measurement circuit diagram is shown in Fig.5(a). To make high-frequency pulsation voltage, DC voltage V_{ds} supplied by DC voltage source and AC voltage v_{ds} outputted by a signal generator. Next, to observe the AC voltage, the ceramic capacitor C_1 for cutting the DC voltage is connected in series with the resistor R_1 and R_x.

Also, Fig.5(a) is based on the idea of the bridge circuit. In the AC equivalent circuit, the bridge circuit is composed of R_1, R_x, C_{gd}, and C_{gs} because C_1 is short and R_2 is much higher impedance than C_{gs}. In addition, to investigate the dependence of V_{gs}, the DC voltage source is connected between the gate and source of MOSFET. In order for this bridge circuit to satisfy the equilibrium condition, the voltage drop of v_x and v_{gs} must be



(a) Measurement circuit diagram for determining the ratio of C_{gd} and C_{gs}.



(b) Measurement circuit diagram for determining C'

Fig.5. Measurement circuit diagram for C_{gd}.

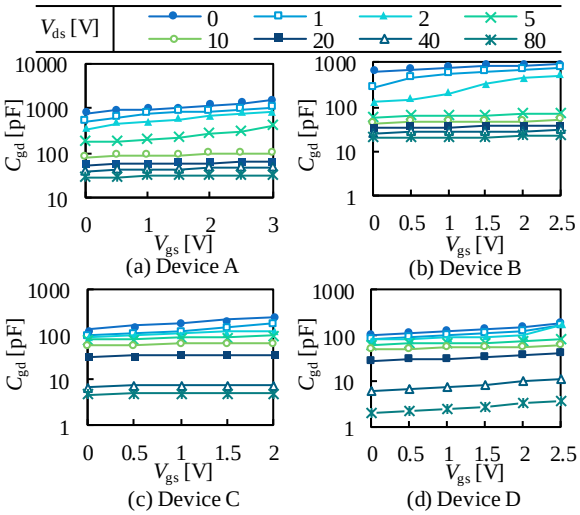


Fig.6. Extracted C_{gd} characteristics.

equal. At this time, the amplitude of v_x and v_{gs} is the same. To satisfy this condition, the variable resistance R_x is adjusted. Finally, we apply the balance condition in this circuit, C_{gd} is obtained as

$$C_{gd} = \frac{R_x}{R_1} C_{gs} . \tag{4}$$

In this paper, this measurement was carried out for DC voltage V_{ds} of 0 to 100V, V_{gs} of 0 to about 3V before the MOSFET turns on and frequency of 1MHz.

Next, another measurement circuit diagram is shown in Fig.5(b). We applied a high-frequency voltage from the impedance analyzer and measured capacitance component. Furthermore, the high impedance resistance 1MΩ is open and

TABLE III. EXTRACTED PARAMETERS OF APPROXIMATE EXPRESSION

Param	Device (S_1)			
	A	B	C	D
A	1640×10^{-9}	1300×10^{-9}	960×10^{-9}	1057.7×10^{-9}
B_1	0.066	0.782	6.4823	0.9961
B_2	1.15	2.072	0.001	0.631
B_3	0.067	0.666	0	0
C	0.0001	0	0.0927	0.0504
D_1	784.7×10^{-9}	850.29×10^{-9}	549×10^{-9}	103.103×10^{-9}
D_2	0	30.88	1.2069	0
E	0.26	0.465	0.8824	0.2166
C_{bias}	25×10^{-9}	20×10^{-9}	4.345×10^{-9}	1.5×10^{-9}

ceramic capacitors 1μF are short in the AC circuit because these have a sufficiently larger capacity than parasitic capacitor of MOSFET. Therefore, the following composite capacitance C' can be measured

$$C' = C_{gs} + \frac{C_{ds}C_{gd}}{C_{ds}+C_{gd}}. \tag{5}$$

Here, the measured value of the curve tracer at the same V_{ds} in section II was adopted as the value of C_{ds}. Therefore, when the ratio R_x/R_1 is k, C_{gs} is obtained as follows from (4) and (5):

$$C_{gs} = \frac{\left[-\left\{(1+k)C_{ds}-kC'\right\}+\sqrt{\left\{(1+k)C_{ds}-kC'\right\}^2+4kC'C_{ds}}\right]}{2k}. \tag{6}$$

Figure 6 shows the measurement results of C_{gd}. As shown in Fig.6, C_{gd} tended to increase as V_{gs} increased. In addition, there was a tendency that the smaller V_{ds}, the stronger dependence of C_{gd} on V_{gs}. Next, to do modeling in PSpice, we carried out a curve fitting from the measurement result using approximate equations. Similar to section II, an external voltage-controlled current source was used in C_{gd} and analog behavior model ABM2/I was used so that we can use the two variables function. Figure 4(b) is the modeling circuit of C_{gd} in the proposed model. This circuit is composed of the editable part and offsets part C_{bias}. The editable part expresses the dependence of v_{ds} and v_{gs}. Also, the editable part composed of two kinds of the capacitor, C_a is used the function of v_{ds}, C_b has used the function of v_{gs}. By connecting these in series, it is possible to describe a two-variable function. When the parameters to be fitted are from A to E, C_a and C_b are expressed by the following approximate expressions:

$$C_a(v_{ds}) = \frac{A}{\left(B_1+B_2v_{ds}+B_3v_{ds}^2\right)}e^{-Cv_{ds}}. \tag{7}$$

$$C_b(v_{gs}) = \left(D_1+D_2v_{gs}\right)e^{Ev_{gs}}. \tag{8}$$

In this paper, we fitted by the solver and each parameter was extracted. This fitting carried out the device in Table I and the extracted parameters are shown in Table III. The modeling

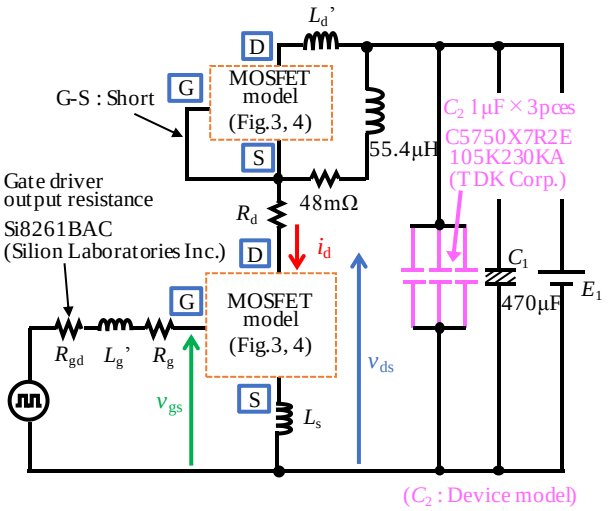


Fig.7. Modeling circuit constructed with PSpice

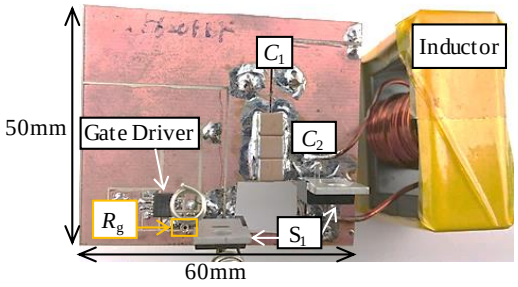


Fig.8. Photograph of the experimental circuit at TO-220 packages.

circuit of MOSFET is Fig.3 and is the same as the conventional model. The circuit diagram of C_{gd} is changed to Fig.4(b). C_a and C_b are collectively expressed using the voltage-controlled current sources ABM2/I with two inputs.

IV. SWITCHING WAVEFORM COMPARISON

In this section, switching waveform is compared with conventional, proposed model and experimental results to evaluate the prediction accuracy of these models. To compare the switching waveforms, we measured by DPT with each S_1.

A. Modeling circuit

Figure 7 shows the modeling circuit of DPT in PSpice. This circuit had a half-bridge structure and was used the same model number MOSFET S_1. Next, S_1 on high-side shorted between the gate and source terminal and the inductor was connected in parallel. C_1 which the high-frequency current flows dominantly and S_1 used the device model of the same model number provided by the manufacturer. Also, we used Si8261BAC (Silicon Laboratories Inc.) as gate driver and output impedance of gate driver R_{gd} has adopted the value in the datasheet [18]. It was 0.8Ω at turn-off and 2.6Ω at turn-on, respectively. Moreover, to reproduce the behavior of gate driver in PCB, the rise and fall times of the pulse voltage applied between the gate and source of low side's S_1 adopted the value of datasheet [18], and were 4.3ns, 9.7ns, respectively.

TABLE IV. THE LIST OF EXPERIMENTAL INSTRUMENTS

Instrument	Part Number (Manufacturer)	Frequency band
Oscilloscope	HDO4034A (Teledyne Lecroy)	350MHz
Passive probe	PP021 (Teledyne Lecroy)	500MHz
Current probe	TCP312 (Tektronix)	100MHz

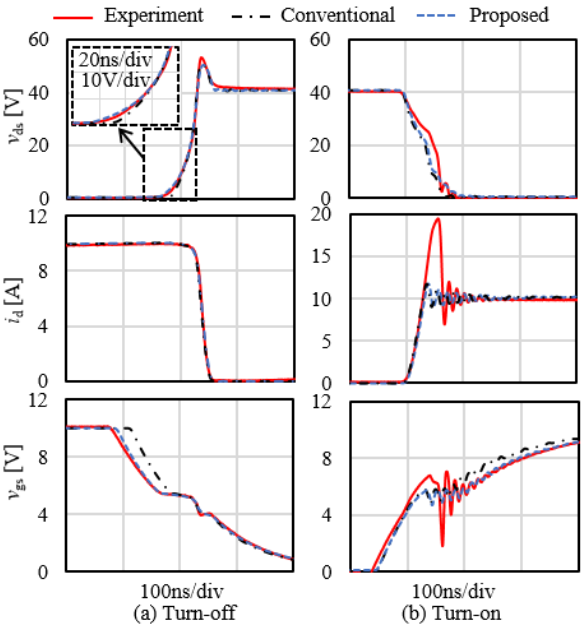


Fig.9. Switching waveform at 40V, 10A, R_g 150Ω, and Device D.

B. Results

Figure 8 shows a photograph of the experimental circuit at TO-220 packages. In this experiment, we supplied the circuit with E_1 of 40V and drain current 10A. However, in the Device C, oscillatory false triggering [17] occurred, so we inserted a small-sized ceramic capacitor between the drain and the gate terminal of it and a U-shaped wire in the experimental PCB, and measured at 20V, 3A. Also, gate resistance R_g was used: 3.3, 10, 33, 68, 100, and 150Ω. Furthermore, the gate voltage of S_1 was set at 10V and applied only two pulses. The first pulse width was determined based on the drain current we wanted to apply to S_1 and we observed turn-off waveform when the first pulse falls. Besides, we observed the turn-on waveform when the second pulse rises.

The list and frequency band of experimental instruments is shown in Table IV. We confirmed that the resonant frequency in the switching waveform didn't exceed the frequency band when we measured the switching waveform.

First, the switching waveforms at R_g of 150Ω and 10Ω for device D, which especially improved the prediction accuracy, are shown in Fig.9 and Fig.10, respectively. The deviations that occurred at the rise of the v_{ds} waveform and the mirror period of v_{gs} waveform in turn-off were improved, and the i_d waveform was almost the same. Therefore, it is considered that the prediction accuracy of turn-off loss is improved. On the other hand, turn-on waveforms didn't almost change. This is thought to be because C_{gd} at turn-on was a smaller contribution to

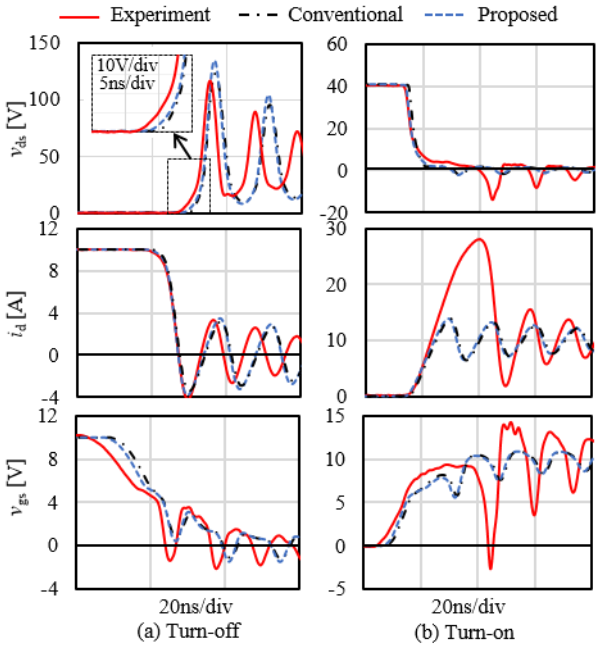


Fig.10. Switching waveform at 40V, 10A, R_g 10Ω, and Device D.

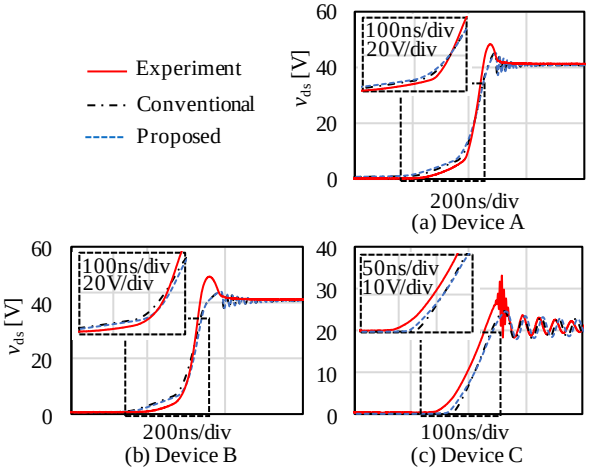


Fig.11. Comparison of v_{ds} waveforms in other devices at R_g 150Ω

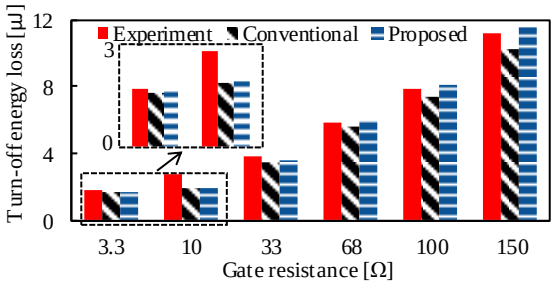


Fig.12. Comparison of turn-off loss of 40V, 10A and Device D

switching waveform than a turn-off. Also, there is a difference in the overshoot of the i_d at turn-on. This difference was attributed to the reverse recovery characteristics of the anti-parallel diode on the high-side, which was not considered in this

model. However, i_d waveform at turn-on from 0 to 10A with adjusted I_d-v_{gs} characteristics shows a good prediction.

Next, Fig.11 shows the v_{ds} waveform at the turn-off of other devices. Device A was almost the same waveform. On the other hand, in device B and C, the slope of the v_{ds} waveform approached the experiment.

Finally, Fig.12 shows the result of comparing the turn-off loss of device D at 40V, 10A. The turn-off loss ranged from the point where v_{ds} rises to 10% of set value to the point where i_d falls to 10% of set value and turn-off loss was dominant in this range. From this figure, similar to the turn-off waveform, it was confirmed that the consideration of the C_{gd} on v_{gs} had a tendency to reduce the deviation from the experiment compared to the no consideration it. From the above, it was revealed that the consideration of the C_{gd} on v_{gs} has the ability to improve the prediction accuracy of the switching waveforms.

V. CONCLUSION

Predicting the switching waveforms is indispensable for future miniaturization and higher density of power conversion circuits. In this paper, we verified the improvement of prediction accuracy by whether or not considering the dependence of the gate-drain capacitance on gate-source voltage. To construct the modeling circuit, we measured wiring parameter and characteristic of the MOSFET. As a result of comparing the switching waveforms, the model considered the dependence of the gate-drain capacitance on gate-source voltage showed that the prediction accuracy of turn-off waveforms tended to improve at the rise of the drain-source voltage and at the fall of the gate-source voltage. Therefore, it was revealed that this consideration has the ability to improve the prediction accuracy of the turn-off waveforms and the turn-off loss.

REFERENCES

[1] P. Dost, P. Spichartz and C. Sourkounis :"Charging Behaviour of Users Utilising Battery Electric Vehicles and Extended Range Electric Vehicles within the Scope of a Field Test," *IEEE 2th Int. Conf. on Renewable Energy Research and Applicat*, (ICRERA), pp.1162-1167, 2015.

[2] Jun Wang, Xiaohu Zhou, Jun Li, Tiefu Zhao, Alex Q. Huang, Robert Calanan, Fatima Husna, and Anant Agarwal, "10-kV SiC MOSFET-Based Boost Converter," *IEEE Trans. Ind. Appl.*, vol. 45, no. 6, pp. 2056–2063, Nov. 2009.

[3] Ryota Maeno, Hideki Omori, Hisato Michikoshi, Noriyuki Kimura, and Toshimitsu Morizane, : "A 3kW Single-Ended Wireless EV Charger with a Newly Developed SiC-VMOSFET," *IEEE 2th Int. Conf. on Renewable Energy Research and Applicat*, (ICRERA), 2018.

[4] J. C. Zolper, "Emerging silicon carbide power electronics components", Proc. *IEEE Appl. Power Electron. Conf.*, (APEC)vol. 1, pp. 11-17, 2015.

[5] Rakesh Ramachandran, and Morten Nymand, "Effectively paralleling GaN FETs to achieve ultra-high efficiency in an isolated DC-DC converter," *IEEE 2th Int. Conf. on Renewable Energy Research and Applicat*, (ICRERA), pp.956-960, 2016.

[6] Yanming Xu, Hong Li, Trillion Q Zheng, Bo Zhao, and Zhe Zhou:"Study on the Pspice simulation model of SiC MOSFET base on its datasheet," *in Proc. IEEE 2nd Int. Future Energy Electron. Conf.* (IFEEC) , pp1-6, 2015.

[7] A. P. Arribas, F. Shang, M. Krishnamurthy, and K. Shenai, "Simple and accurate circuit simulation model for SiC power MOSFETs," *IEEE Trans. Electron Devices*, vol. 62, no. 2, pp. 449–457, Feb. 2015.

[8] Yuming Zhou, Hangzhi Liu, Tingting Yang, and Bing Wang, "SPICE Modeling of SiC MOSFET Considering Interface-Trap Influence", *CPSS Trans. on Power Enectron. and Appl*., Vol.3, No.1, March 2018.

[9] Duan Zhuolin, Zhang Dong, Fan Tao, and Wen Xuhui : "A simple SiC power MOSFET model" , *43rd Annu. Conf. of the IEEE Ind. Electron. Soc.* (IECON), pp704-708, 2017.

[10] Yasushige Mukunoki , Yuta Nakamura, Kentaro Konno, Takeshi Horiguchi, Yasushi Nakayama, Akinori Nishizawa, Masaki Kuzumoto, and Hirofumi Akagi : "Modeling of a Silicon-Carbide MOSFET With Focus on Internal Stray Capacitances and Inductances, and Its Verification" , *IEEE Trans. Ind. Appl.*, Vol.54, no.3, pp2598-2597, 2018.

[11] Hiroyuki Sakairi, Tatsuya Yanagi, Hirotaka Otake, Naotaka Kuroda, Hiroaki Tanigawa, and Ken Nakahara : "Measurement Methodology for Accurate Modeling of SiC MOSFET Switching Behavior Over Wide Voltage and Current Ranges", *IEEE Trans. on Power Electron.*, Vol.33, no.9, pp7314 - 7325, Sept. 2018.

[12] Z. Chen, D. Boroyevichn, and R Borgos : "Experimental Parasitic Study of the Parasitic Inductance Influence on MOSFET Switching Charateristics" , *European Conf. on Power Electron. and Applicat.* (EPE), pp.1-9, 2017.

[13] Yanqun shen, Jian Jiang, Yan Xiong, Yan Deng; Xiangning He, Zhaohui Zeng : " Parasitic Inductance Effects on the Switching Loss Measurement of Power Semiconductor Devices" , *IEEE Int. Symp. on Ind. Electron.* (ISIE), pp.847-852, 2006.

[14] Zezheng Dong, Xinke Wu, Kuang Sheng, Junming Zhang : "Impact of common source inductance on switching loss of SiC MOSFET" , *IEEE 2nd Int. Future Energy Electron. Conf.* (IFEEC), pp1-5, 2015.

[15] K. Aikawa, T. Shiida, R. Matsumoto, K. Umetani, and E. Hiraki : "Measurement of the common source inductance of typical switching device packages," in Proc. *IEEE Int. Future Energy Electron. Conf.* (IFEEC), pp.1–6, 2017.

[16] K. Umetani, K. Aikawa, and E. Hiraki, : "Straightforward measurement method of common source inductance for high speed switching semiconductor devices mounted on-board," *IEEE Trans. Ind. Electron.*, Vol. 64, No.10, pp. 8258–8267, Jan.-Feb. 2017.

[17] K. Umetani, R. Matsumoto, and E. Hiraki, : "Prevention of Oscillatory False Triggering of GaN-FETs by Balancing Gate-Drain Capacitance and Common-Source Inductance," *IEEE Trans. Ind. Appl*., Vol. 55, No.1, pp. 610-619, Oct. 2019.

[18] Sillicon Laboratories, "Si8261BAC datasheet," pp4-6, 2013