Parasitic inductance design for preventing oscillatory false triggering of parallel-connected GaN-FETs

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Parasitic Inductance Design for Preventing Oscillatory False Triggering of Parallel-Connected GaN-FETs

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***Abstract*—GaN-FETs are recently spreading in high-power switching converters, where GaN-FETs are commonly parallel connected to switch the large current. However, the parallel-connected GaN-FETs often suffer from false triggering because the parallel connection incorporates multiple LC resonators of the parasitic capacitance of GaN-FETs and the parasitic inductance of the printed circuit board, which can be easily excited by the switching noise and fluctuate the gate voltage. Particularly, GaN-FETs are susceptible to the self-sustaining repetition of the false triggering, i.e. the oscillatory false triggering, which must be prevented in industrial products. For prevention of this phenomenon in the case of a single GaN-FET, the preceding studies have proposed the design instruction of the parasitic inductance. However, few insights are available for the parallel-connected GaN-FETs. The purpose of this paper is to elucidate the design instruction to prevent the oscillatory false triggering for parallel-connected GaN-FETs through analyzing the equivalent circuit model of this phenomenon. The result revealed that parallel-connected GaN-FETs need the design instruction slightly modified from that for a single GaN-FET. The appropriateness of this modified instruction was verified by the simulation, suggesting the feasibility of this instruction for applying the parallel-connected GaN-FETs in high-power switching converters.**

Keywords—common-source inductance, false triggering, GaN-FET, oscillatory false triggering, parasitic inductance.

I. Introduction

GaN-FETs are emerging as a promising device for efficiency improvement of power converters owing to low conduction loss and high-speed switching performance [1][2]. The maximum current rating of the currently available GaN-FETs is still limited to several tens of amperes. Therefore, the GaN-FETs have been mainly adopted for the low-power switching converters. However, GaN-FETs are recently spreading to the high power applications, in which GaN-FETs are parallel connected to increase the current rating [3]–[7].

Nonetheless, parallel-connected GaN-FETs are especially susceptible to false triggering, which hinders practical applications of GaN-FETs in high-power applications. The reason for this susceptibility is originated from the two reasons. One is that GaN-FETs generally have a low gate threshold voltage compared to the conventional silicon MOSFETs. The other is that the fast switching capability of the GaN-FETs will generate a large switching noise, particularly when it switches the large current in high power applications.

The switching noise is the voltage drop across the parasitic inductance of the printed circuit board (PCB) wiring or the semiconductor package constituting the power circuit, caused by the sudden change in the drain current at the switching operation. This switching noise is superimposed on the gate voltage due to the drain-gate capacitance C_{gd} and the parasitic inductance of the source terminal L_s of the switching device, leading to false triggering. Therefore, reduction of the parasitic inductance of the power circuit, as well as reduction of C_{gd} and L_s, has been conventionally sought for preventing false triggering.

A number of studies have been dedicated to proposing the PCB design for avoiding false triggering both in a single switching device [8]–[11] and parallel-connected switching devices [5]. These studies have elucidated that PCB design with less parasitic inductance is effective for preventing the normal false triggering, which is the non-repetitive false triggering caused by the self-decaying gate voltage fluctuation induced by the switching noise, such as the self-turn-on [12]. However, recent studies have pointed out that reduction of the parasitic inductance is not necessarily effective for preventing another type of false triggering, called the oscillatory false triggering.

The oscillatory false triggering is a peculiar phenomenon of GaN-FET, appearing as the self-sustaining repetition of false triggering triggered by the switching [13]–[16]. The oscillatory false triggering causes the enormous switching loss accompanied by the huge number of the switching. Therefore, this phenomenon is particularly disastrous and must be solved for practical industrial products.

According to the preceding studies [13]–[16], the oscillatory false triggering is caused by the parasitic oscillator circuit comprised of the GaN-FET, the parasitic capacitance of the GaN-FET, and the parasitic inductance of the PCB. Therefore, the oscillatory false triggering can be prevented by the optimal design of the parasitic inductance

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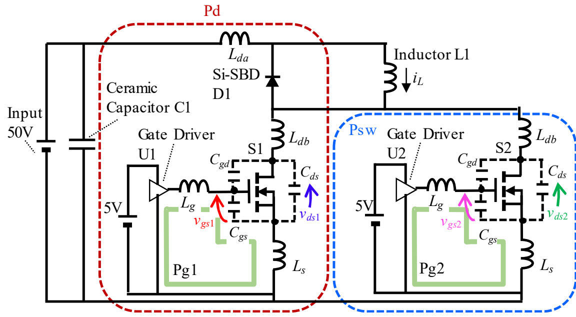
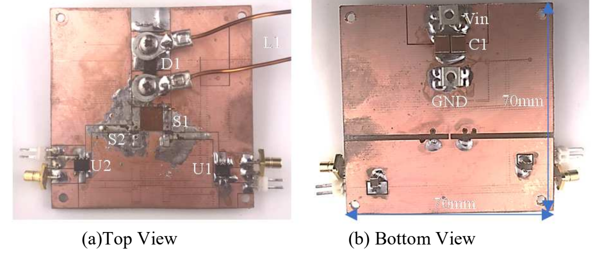


Fig. 1. Circuit diagram of single pulse test circuit.



(a)Top View (b) Bottom View

Fig. 2. Photographs of single pulse test circuit.

TABLE I. SPECIFICATIONS OF SINGLE PULSE TEST CIRCUIT

S1,S2	GaN-FET EPC2207 (EPC Corp.)
D1	Si-SBD V10P10-M3/86A (Vishay Semiconductors)
C1	Ceramic Capacitor 22uF×2pcs CKG57NX7S2A226M500JH (TDK Corp.)
L1	30uH N49 Ferrite core inductor
U1,U2	Gate Driver NCP81074ADR2G (ON Semiconductor)

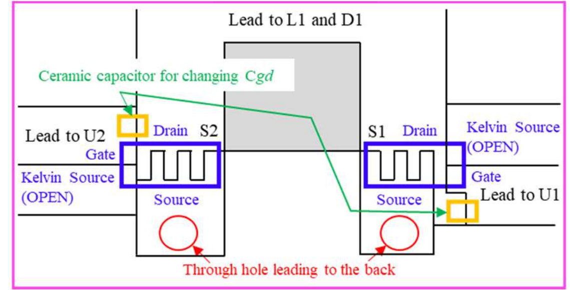


Fig. 3. PCB Layout of single pulse test circuit near GaN-FETs

such that the parasitic oscillator circuit does not meet the oscillation condition. In the case of a single GaN-FET, [15][16] has succeeded to formulate the required condition of the parasitic inductance to prevent the oscillatory false triggering. However, parallel-connection of GaN-FETs incorporates more complicated networks of the parasitic capacitance of these GaN-FETs and the parasitic inductance of wiring paths of the PCB than a single GaN-FET. Accordingly, no design instruction of the parasitic inductance has been proposed in the case of the parallel-connected GaN-FETs, to the best of the authors' knowledge.

The purpose of this paper is to elucidate the design instruction of the parasitic inductance for parallel-connected GaN-FETs through analyzing the equivalent circuit model of the oscillatory false triggering in parallel-connected GaN-FETs. Similarly as in the previous study [15][16], this paper firstly constructs the high-frequency ac equivalent circuit model of the parasitic oscillator circuit comprised of the parasitic inductance and capacitance as well as the switching device. Then, based on this model, this paper derives the requirement for preventing the oscillatory false triggering.

The following discussion is organized into five sections. Section II reports the oscillatory false triggering of parallel-connected GaN-FETs observed in an experiment. Section III constructs the equivalent circuit model of the parasitic oscillation circuit incorporating parallel-connected GaN-FETs and derives the proposed design instruction of the parasitic inductance for preventing the oscillatory false triggering. Then, sections IV and V present the simulation and experimental results, respectively, to test the proposed design instruction. Finally, section VI gives the conclusions.

II. EXPERIMENTAL WAVEFORMS OF OSCILLATIONALY FALSE TRIGGERING OF PARALLEL-CONNECTED GAN-FETS

An experiment was carried out to observe the oscillatory false triggering of parallel-connected GaN-FETs. For this purpose, a single pulse test circuit shown in Fig. 1 was employed to observe the turn-off operation of the GaN-FETs. Table I shows the list of the circuit elements of the test circuit. Figure 2 shows the photographs of the single pulse test circuit. The test circuit comprises the half-bridge circuit of Si Schottky barrier diode D1 and the parallel connection of GaN-FETs S1 and S2. Each of S1 and S2 is driven by its gate driver IC. No external gate resistor was connected to achieve as fast switching as possible. The half-bridge circuit was supplied with the DC voltage via the decoupling capacitor C1. L1 was an inductor attached in parallel to D1.

Inductance L_{da}, L_{db}, L_s, and L_g are the parasitic inductance of the PCB layout, whereas capacitance C_{gd}, C_{gs}, and C_{ds} are the parasitic capacitance of S1 and S2. L_{da} represents the inductance of the power loop path Pd except for the wiring paths that are separated between S1 and S2. L_{db} represents the inductance of these separated wiring paths. L_s represents the inductance of the source terminal, which is called the common source inductance [18]. L_g represents the parasitic inductance of the gate loop paths, notated Pg1 and Pg2. The pattern layout of the PCB, depicted in Fig. 3, was designed to be as symmetrical between S1 and S2 as possible, which is pointed out to be an elementary remedy for reducing the possibility of the false triggering in the preceding study [5]. Therefore, the parasitic inductance is expected to take the symmetrical values.

By utilizing the measurement method of the parasitic inductance described in [15][16], the inductance of the power loop path Pd was measured as 11.7 nH; the inductance of the gate loop paths Pg1 and Pg2 were measured as 12.0 nH and 13.1 nH, respectively; the inductance of the loop path between S1 and S2, notated as Psw, was measured as 10.6 nH. Furthermore, the common source inductance L_{s1} and L_{s2} of switching device S1 and S2, were measured as 0.72 nH and 0.58 nH, respectively, according to the measurement method described in [20]. If L_{g1} and L_{g2} denotes the parasitic inductances of the gate loop paths of S1 and S2, respectively, the inductance of Pd, Pg1, Pg2 and Psw can be expressed as L_{da}+(L_{db}+L_{s1})//(L_{db}+L_{s2}), L_{g1}+L_{s1}, L_{g2}+L_{s2} and 2L_{db}+L_{s1}+L_{s2}. (The common source inductance of S1 and S2, i.e. L_{s1} and L_{s2}, were both represented as L_s in Fig. 1. Similarly, both L_{g1} and L_{g2} were represented as L_g in Fig. 1.) Consequently, L_{da}, L_{db}, L_{g1} and L_{g2} were determined to be 9.1 nH, 4.6 nH, 11.3 nH and 12.5 nH, respectively, considering that the GaN-FETs under test have the flip-chip package and therefore has extremely small parasitic inductance of package.

TABLE II. LIST OF EXPERIMENTAL INSTRUMENTS

Instrument	Model (Manufacturer)	Frequency limit
Oscilloscope	TPS2024 (Tektronix)	200MHz
Passive Probe	P6139B (Tektronix)	500MHz

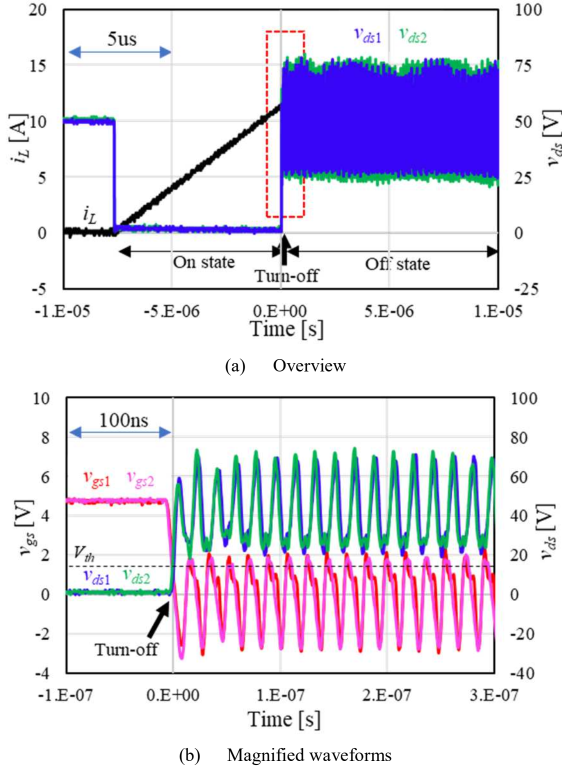


Fig. 4. Voltage waveforms just after the turn-off.

As pointed out in the previous studies on the oscillatory false triggering [16], the occurrence of the oscillatory false triggering is highly dependent on C_{gd} and L_s. Therefore, in this experiment, C_{gd} was increased from its natural value of S1 and S2 by 39 pF to conveniently cause the oscillatory false triggering. For this purpose, a small ceramic capacitor of 39 pF was attached directly between the gate and drain terminals of S1 and S2 because the GaN-FETs under test have a small parasitic inductance of the package. Meanwhile, the value of L_s was not adjusted because L_s has an extremely small value, and therefore adjusting L_s would require an extremely delicate design of the PCB layout as exemplified in [17].

In this experiment, the two GaN-FETs were first turned on simultaneously to charge inductor L1 with the current. Then, after the current of L1 reaches approximately 12 A, these GaN-FETs were turned off simultaneously. Then, the drain-source voltage and the gate-source voltage of these two GaN-FETs were observed after the turn-off. Table II lists the measurement instruments employed in the experiment.

Figure 4 shows the results. As can be seen in Fig. 4(a), the high-frequency sustaining oscillation occurred in the drain-source voltage of S1 and S2, i.e. v_{ds1} and v_{ds2}, after the turn-off. Figure 4(b) shows the magnified voltage waveforms of this oscillation just after the turn-off. The gate-source voltage of S1 and S2, i.e. v_{gs1} and v_{gs2}, also exhibited the high-frequency oscillation with the same frequency as that of v_{ds1} and v_{ds2}. This oscillation has an amplitude greater than the gate threshold voltage; the timing of the peaks in v_{gs1} and v_{gs2} coincides with the timing of the valleys in v_{ds1} and v_{ds2}, which indicates that this oscillation accompanies a huge number of false triggering of the GaN-FETs.

As pointed out in [15][16], these features imply that this oscillation is caused as a result of the linear physical mechanism. In fact, [15][16] have proven that the oscillatory false triggering can be modeled as the linear oscillation circuit model. Therefore, the design instruction for preventing the oscillatory false triggering of parallel-connected GaN-FETs can be derived by investigating the non-oscillatory condition of a linear oscillation circuit model.

III. ANALYSIS OF OSCILLATION CIRCUIT MODEL

This section derives the design instruction of the parasitic inductance to prevent the oscillatory false triggering in parallel-connected GaN-FETs by constructing and analyzing the equivalent circuit model of the oscillatory false triggering. This equivalent circuit model is constructed based on the experimental single pulse test circuit shown in the previous section to model the high-frequency ac oscillation observed immediately after the turn-off of the two GaN-FETs. The equivalent circuit is assumed to be linear for simplifying the analysis because the voltage waveforms observed in the previous section implied that the oscillatory false triggering has the linear mechanism and therefore the linear equivalent circuit can be expected to model the basic feature of the oscillatory false triggering.

A. Model Construction

This subsection constructs the high-frequency equivalent circuit model based on Fig. 1. After the turn-off of the two GaN-FETs, the dc current flows through diode D1 and therefore D1 has a small ac resistance for the oscillation current. Hence, D1 is simply regarded as the short-circuit in the equivalent circuit model.

As observed in the previous section, the oscillatory false triggering occurred at a high frequency where the parasitic capacitance of the switching device and the parasitic inductance of the PCB takes an essential role. Therefore, these parasitic elements should be included in the equivalent circuit. (The parasitic capacitance of the switching device is approximated to be constant regardless of the voltage across the capacitance to obtain the linear equivalent circuit.) However, the parasitic resistance in the circuit is neglected to simplify the analysis. This corresponds to the worst case, in which no damping exists for the oscillation in the equivalent circuit. Therefore, the non-oscillatory condition obtained under this approximation is valid also under the existence of the parasitic resistance, because the analysis of the equivalent circuit will yield a sufficient condition to prevent the oscillatory false triggering.

The impedance of the decoupling capacitor can be neglected compared to that of the parasitic capacitance of the switching device as well as the parasitic inductance of the PCB layout. Hence, the decoupling capacitors are regarded as short circuits. Contrarily, inductor L1 has a far larger impedance than the parasitic inductance and capacitance. Hence, this inductor is regarded as an open circuit.

Consequently, the experimental circuit, i.e. Fig. 1, yields the ac equivalent circuit shown in Fig. 5. Inductance L_{da}, L_{db}, L_g, and L_s represent the parasitic inductance of the PCB including the parasitic inductance of the switching device

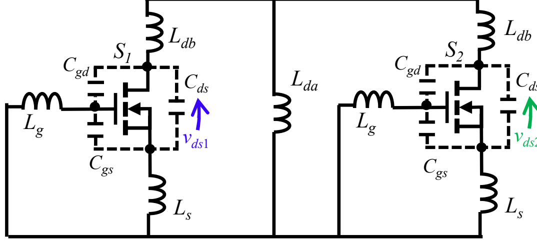


Fig. 5. Equivalent circuit of oscillatory false triggering of two parallel-connected GaN-FETs.

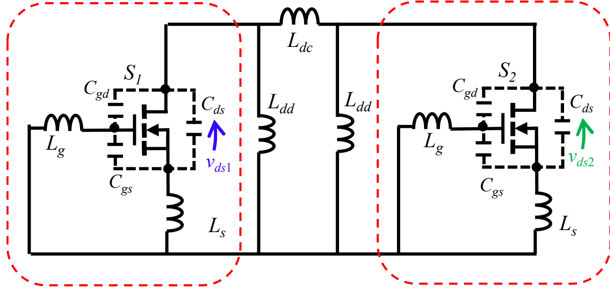


Fig. 6. Modified equivalent circuit of Fig. 5.

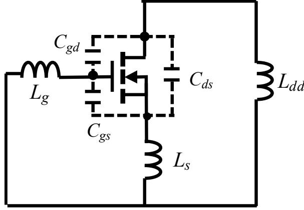


Fig. 7. Independent oscillation circuit block in Fig. 6.

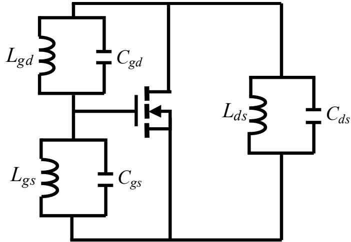


Fig. 8. Final equivalent circuit model.

package; C_{ds}, C_{gs}, C_{gd} represent the drain-source capacitance, gate-source capacitance, and gate-drain capacitance of the GaN-FET, respectively.

Next, Fig. 5 is transformed into another equivalent circuit to simplify the analysis. Applying the Y-Δ transformation to the Y-connection of the parasitic inductance L_{da} and L_{db} yields the modified equivalent circuit shown in Fig. 6, where L_{dc} and L_{dd} are defined as

$$L_{dc} = 2L_{db} + \frac{L_{db}^2}{L_{da}}, \quad L_{dd} = 2L_{da} + L_{db}. \tag{1}$$

B. Oscillation condition analysis

The equivalent circuit of Fig. 6 has a symmetrical topology made of the same circuit blocks, which are marked by the red dashed line, connected by L_{dc}. Because the same gate signal is supplied to both of the two circuit blocks, the two circuit blocks operate symmetrically and therefore no voltage difference is applied between the two terminals of L_{dc}. Consequently, no current is flowing through $L_{dc,}$ and therefore each circuit block can be regarded to operate independently.

Now, the analysis of the equivalent circuit is reduced to the analysis of the independent circuit block shown in Fig. 7. This block has the same topology but with different values of parameters as the parasitic oscillator circuit analyzed in [16], which derived the requirement of the parasitic inductance for preventing the oscillatory false triggering in the case of a single GaN-FET. Therefore, the same procedure can be taken for analyzing Fig. 7. Hereafter, this procedure is followed to derive the requirement for preventing the oscillatory false triggering of parallel-connected GaN-FETs.

Figure 7 contains the Y-connection of L_{dd}, L_g, and L_s. Therefore, again applying the Y-Δ transformation yields the final equivalent circuit shown in Fig. 8, where L_{gd}, L_{gs}, and L_{ds} are the inductance defined as

$$L_{gd} = \frac{L_p}{L_s}, \quad L_{gs} = \frac{L_p}{L_{dd}}, \quad L_{ds} = \frac{L_p}{L_g}, \quad L_p = L_g L_s + L_g L_{dd} + L_s L_{dd}. \tag{2}$$

This resultant equivalent circuit can be classified as the Barkhausen-type oscillator [19]. According to the analysis shown in [16], the sufficient condition to prevent the oscillation is derived as

$$\frac{L_{dd}}{C_{gs}} < \frac{L_s}{C_{gd}} < \frac{L_g}{C_{ds}} \quad \text{or} \quad \frac{L_g}{C_{ds}} < \frac{L_s}{C_{gd}} < \frac{L_{dd}}{C_{gs}}. \tag{3}$$

The result indicates that the ratio of L_s to C_{gd} has the appropriate range for preventing the oscillation, i.e. the oscillatory false triggering. Specifically, this ratio should be designed between L_{dd}/C_{gs} and L_g/C_{ds}.

This instruction to prevent the oscillatory false triggering in parallel-connected GaN-FETs is closely similar to that in a single GaN-FET, derived in [16]. However, the value of the appropriate range of L_s/C_{gd} is slightly different from the case of a single GaN-FET. In fact, according to [16], the design instruction of L_s/C_{gd} to prevent the oscillatory false triggering was proposed as follows, if only S1 is mounted and S2 is unmounted in Fig. 1.

$$\frac{L_{da}+L_{db}}{C_{gs}} < \frac{L_s}{C_{gd}} < \frac{L_g}{C_{ds}} \quad \text{or} \quad \frac{L_g}{C_{ds}} < \frac{L_s}{C_{gd}} < \frac{L_{da}+L_{db}}{C_{gs}}. \tag{4}$$

Comparison between (3) and (4) indicates that the inductance of the power loop inductance Pd, i.e. L_{da}+L_{db}, in the design instruction for a single GaN-FET is replaced by $2L_{da}$+L_{db} in that for parallel-connected GaN-FETs. Therefore, parallel-connected GaN-FETs may suffer from the oscillatory false triggering, even if a single GaN-FET does not experience this problem with the same PCB layout. Consequently, the PCB design for parallel-connected GaN-FETs must consider the parasitic inductance design instruction specialized for parallel-connected GaN-FETs, i.e. the proposed instruction formulated as (3).

IV. Simulation

A simulation was carried out to test the proposed design instruction, i.e. (3). In this simulation, the single pulse test circuit shown in Fig. 1 was constructed in the model space of OrCAD Pspice ver. 17.2. The occurrence of the oscillatory false triggering was tested under various values of L_s and C_{gd} to identify the appropriate range of L_s/C_{gd}. Then, the identified range of L_s/C_{gd} was compared between the simulation and the proposed design instruction, as well as between the case of parallel-connected GaN-FETs and the case of a single GaN-FETs.

Figure 9 shows the simulation circuit model. The inductors in the model represent the parasitic inductance of the PCB layout, except for the 20μH inductor representing L1 in Fig. 1. The parasitic inductances were designed to be symmetrical between S1 and S2. Parasitic capacitances of S1 and S2, as well as diode D1, were incorporated in the Spice device models. However, additional capacitors were attached between the gate and the drain of S1 and S2 to vary the value of C_{gd}. (These additional capacitors have the same capacitance between S1 and S2.)

The Spice models of S1 and S2 were the device models of EPC2207 supplied by EPC Corp. The spice model of D1 was the device model of SBR10U200P5-13 supplied by Diode Detex Corp. The two GaN-FETs, i.e. S1 and S2, were driven with the same gating signal supplied by the rectangular pulse voltage generator. This pulse voltage generator generates the signal whose top and bottom voltage were 5V and −1V, respectively.

The single pulse test circuit was operated similarly as in section II. First, S1 and S2 were kept in the on-state until the 20μH inductor current reaches 20A. Then, S1 and S2 were turned off simultaneously to observe the drain-source and gate-source voltage waveforms after the turn-off and investigate the occurrence of the oscillatory false triggering. This process was repeated under various values of L_s and C_{gd} to identify the occurrence condition of the oscillatory false triggering.

Figures 10 and 11 present the simulation results of the oscillatory false triggering and normal switching without false triggering of parallel-connected GaN-FETs, respectively. Figure 10 was observed when L_s=0.6 nH and C_{gd}=15 pF, whereas Fig. 11 was observed when L_s= 0.8 nH and C_{gd}= 15 pF. Therefore, the difference between Figs. 10 and 11 lie in only a small difference in L_s.

Because the simulated circuit was perfectly symmetrical between S1 and S2, the operation waveforms of the drain-gate voltage (v_{ds}), the gate-source voltage (v_{gs}), and the drain current (i_d) were the same between S1 and S2. In Fig. 10, the continuous oscillation was found in v_{ds}, v_{gs}, and i_d at the frequency of 77 MHz, just after the turn-off. In this oscillation, the peaks of v_{gs} exceeded the gate threshold voltage, which is identical to 1.4V, and the timings of the peaks in v_{gs} coincided with the timings of the valleys in v_{ds}. This feature is consistent with the oscillatory false triggering observed experimentally in section II. Meanwhile, in Fig. 11, the gate-source voltage of both S1 and S2 was kept below the gate threshold voltage after the turn-off and therefore the turn-off switching experienced no false triggering. Therefore, a slight difference in L_s resulted in this drastic difference in the switching.

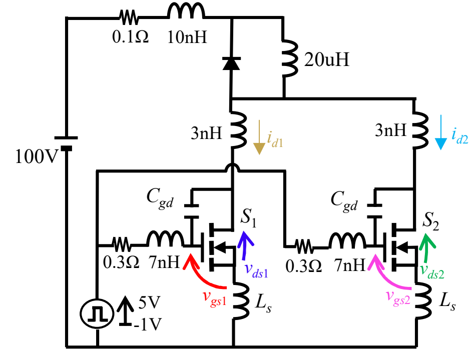


Fig. 9. Pspice simulation circuit model

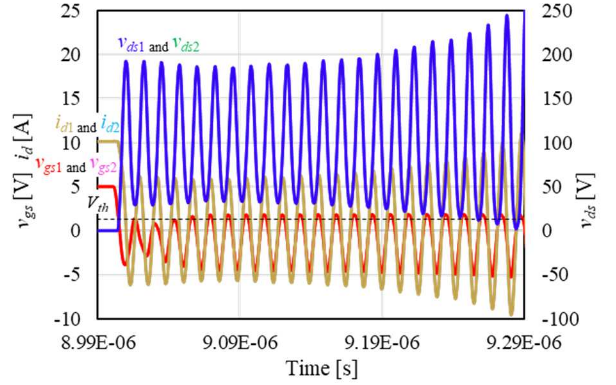


Fig. 10. Simulated turn-off waveforms of parallel-connected GaN-FETs when L_s=0.6 nH and C_{gd}=15pF.

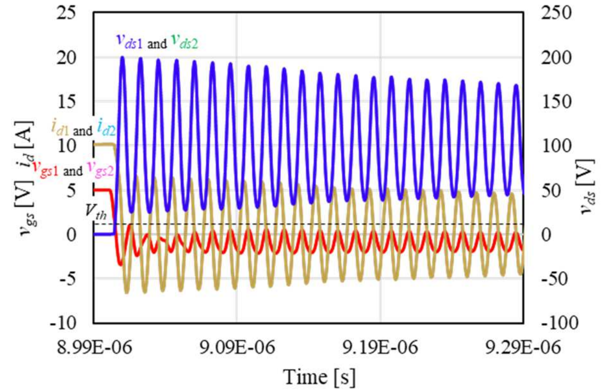


Fig. 11. Simulated turn-off waveforms of parallel-connected GaN-FETs when L_s=0.8 nH and C_{gd}=15pF.

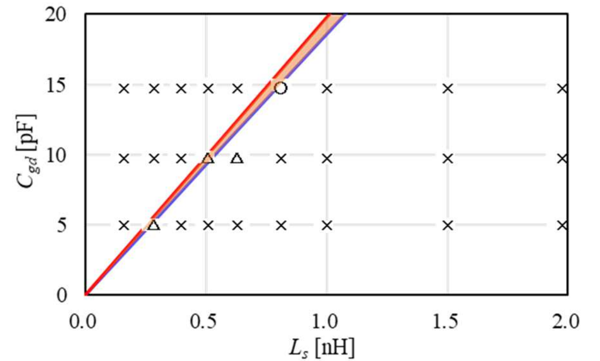


Fig. 12. Simulation result of the occurrence of false triggering of parallel-connected GaN-FETs. Marks '×', 'Δ', and '○' represent the oscillatory false triggering, the false triggering less than 10 times, and the normal switching without false triggering, respectively.

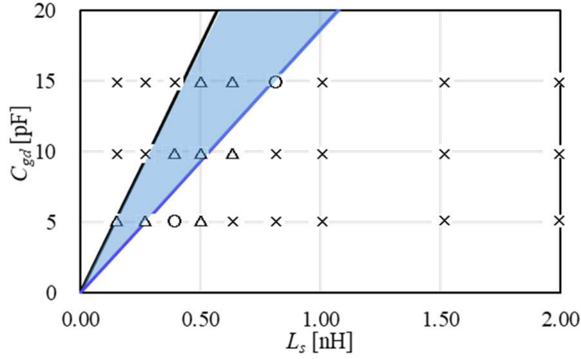


Fig. 13. Simulation result of the occurrence of false triggering when S1 is mounted and S2 is unmounted. Marks '×', 'Δ', and '○' represent the oscillatory false triggering, the false triggering less than 10 times, and the normal switching without false triggering, respectively.

Figure 12 plots the occurrence of the oscillatory false triggering of parallel-connected GaN-FETs in various values of C_{gd} and L_s. The region highlighted by red is the analytically predicted condition of C_{gd} and L_s where the oscillatory false triggering is expected to be prevented according to (3). On the other hand, marks '×', 'Δ', and '○' represent the oscillatory false triggering, the false triggering less than 10 times, and the normal switching without false triggering, respectively. As can be seen in the figure, the simulation results well supported the theoretical prediction by (3), supporting the appropriateness of the proposed parasitic inductance instruction.

Next, to compare the occurrence condition of the oscillatory false triggering between the case of parallel-connected GaN-FETs and the case of a single GaN-FET, an additional simulation was also performed under the condition when only S1 is mounted and S2 is unmounted. Figure 13 shows the occurrence of the oscillatory false triggering in various values of C_{gd} and L_s when only S1 is mounted. The region highlighted by blue represents the analytically predicted condition of C_{gd} and L_s where the oscillatory false triggering is expected to be prevented according to [16]. Marks '×', 'Δ', and '○' represent the simulation results. As can be seen in the figure, the simulation results well supported the theoretical prediction by [16]. However, a comparison between Fig. 12 and Fig. 13 indicates that the condition of C_{gd} and L_s where the oscillatory false triggering does not exist is different between the case of parallel-connected GaN-FETs and the case of a single GaN-FET. Consequently, the simulation results suggest that the PCB design for parallel-connected GaN-FETs needs to follow a different parasitic inductance design instruction specialized for parallel-connected GaN-FETs, as is consistent with the analysis results.

V. Experiment

An experiment was carried out to verify the proposed design instruction formulated as (3), which predicted the parasitic inductance design instruction specialized for parallel-connected GaN-FETs. This experiment employed the same signle pulse test circuit with the same circuit elememts as in section II. However, this experiment changed C_{gd} to various capacitance values to evaluate the occurrence dependence of the oscillatory false triggering on L_s/C_{gd}. Capacitance C_{gd} of each S1 and S2 was varied by adding a small sized ceramic capacitor directly mounted between the drain and gate terminals. The experimentally determined occurrence dependence of the oscillatory false triggering is then compared between the case of parallel-connected GaN-FETs, in which both S1 and S2 are mounted, and the case of a single GaN-FET, in which only S1 is mounted and S2 is unmounted. The inductance values in the case of parallel-connected GaN-FETs is the same as described in section II: L_{da}, L_{db}, L_{g1} and L_{g2} were determined to be 9.1 nH, 4.6 nH, 11.3 nH and 12.5 nH, respectively. In the case of a single GaN-FET, L_{g1} and L_{g2} were the same as the other case, although L_{da}+L_{db}, which is identical to the subtraction of L_{s1} from the parasitic inductance of the loop wiring path Pd, was measured as 16.1 nH. The reason for the difference in L_{da}+L_{db} between the two cases is not cleared in the paper. However, this may be caused by the mutual inductance among the wirings of the power loop path considering that the parasitic inductance network illustrated in Fig. 1 does not incorporate the mutual inductance.

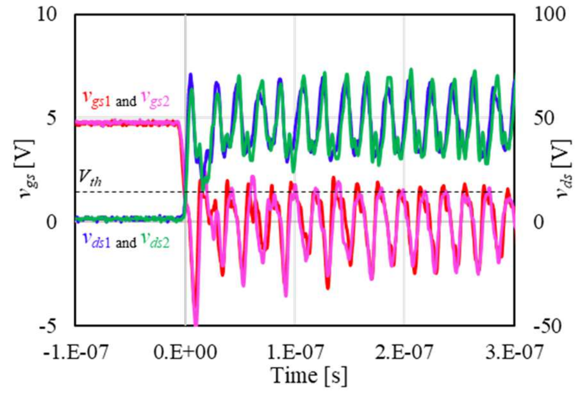


Fig. 14. Experimental turn-off waveforms of parallel-connected GaN-FETs when C_{gd}=49 pF.

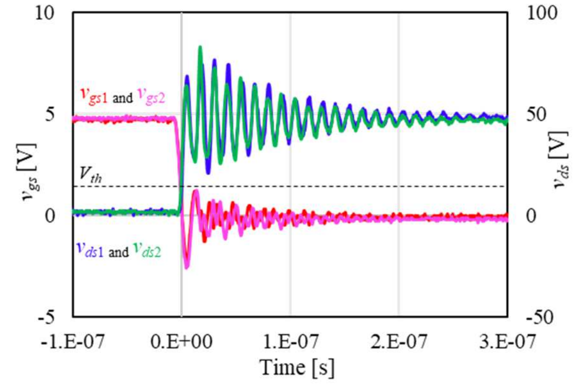


Fig. 15. Experimental turn-off waveforms of parallel-connected GaN-FETs when C_{gd}=12 pF.

Figure 14 shows the switching waveforms with the oscillatory false triggering in the case of parallel-connected GaN-FETs, which was observed at C_{gd}=49 pF. (Figure 4 shows the waveforms of a different condition, which was observed at C_{gd}=41 pF.) On the other hand, Fig. 15 shows the switching waveforms of the normal switching of parallel-connected GaN-FETs without the false triggering, which was observed at C_{gd}=12 pF. As can be seen in these figures, the difference in C_{gd} can significantly affects the occurrence of the oscillatory false triggering, as is expected from the theoretical anlaysis in section III.

Figures 16 and 17 show the evaluation results of the occurrence of the oscillatory false triggering in the case of parallel-connected GaN-FETs and a single GaN-FET, respectively. These figures plot the occurrence with the horizontal axis representing L_s and the vertical axis representing C_{gd}. The triangular red area of Fig. 16 shows the theoretically predicted area of the non-occurrence of the oscillatory false triggering according to the proposed design instruction for parallel-conneted GaN-FETs, i.e. (3). On the other hand, the triangular blue area of Fig. 17 shows the theoretically predicted area of the non-occurrence of the oscillatory false triggering according to the preceding desing instruction for a single GaN-FET, i.e. (4). Therefore, the region of non-occurrence of the oscillatory false triggering was smaller in the case in which both S1 and S2 were mounted. The marks '×', 'Δ', and '○' have the same meanings as in Fig. 12 and Fig. 13. As can be seen in Fig. 16 and Fig. 17, mark '○', which represents the normal switching without false triggering, agreed well with the theoretically predicted condition for the non-occurrence of the oscillatory false triggering.

Certainly, mark 'Δ' should also be classified to the non-occurrence of the oscillatory false triggering because this mark represents the non-sustaining false triggerings less than 10 times. Therefore, the experimentally observed range of C_{gd} for the non-occurrence of the oscillatory false triggering slightly exceeded the theoretically predicted range. The reason of this discrepancy lies in the fact that the theoretical prediction corresponds to the sufficient condition for the non-occurrence of the oscillatory false triggering. However, the experimentally observed non-occurrence range of the oscillatory false triggering was smaller in the case of parallel-connected GaN-FETs than the case of a single GaN-FET, similarly to the theoretaically predicted non-occurrence range, thus supporting the theoretical analysis in section III.

Consequently, the experiment also supported the proposed design instruction, suggesting that the PCB design for parallel-connected GaN-FETs needs to follow a different parasitic inductance design instruction specialized for parallel-connected GaN-FETs

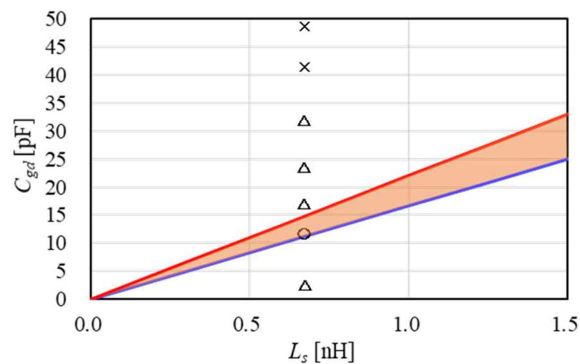


Fig. 16. Exprimental result of the occurrence of false triggering of parallel-connected GaN-FETs. Marks '×', 'Δ', and '○' represent the oscillatory false triggering, the false triggering less than 10 times, and the normal switching without false triggering, respectively.

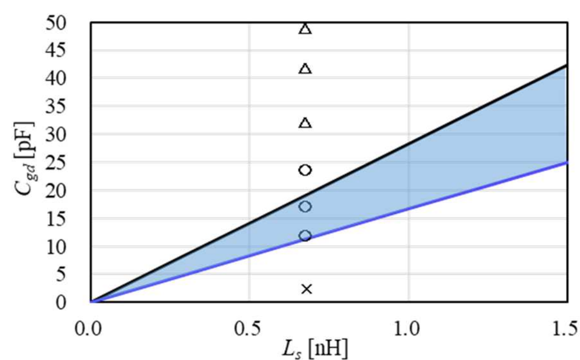


Fig. 17. Experimental result of the occurrence of false triggering when S1 is mounted and S2 is unmounted. Marks '×', 'Δ', and '○' represent the oscillatory false triggering, the false triggering less than 10 times, and the normal switching without false triggering, respectively.

VI. Conclusions

The oscillatory false triggering is one of the major issues to be solved for the industrial application of GaN-FETs. Particularly, parallel-connected GaN-FETs, which are commonly utilized in high power applications to switch the large current, tend to suffer from the oscillatory false triggering due to the large switching noise generated by the high current switching. To solve this problem, this paper analytically derived the parasitic inductance design instruction to prevent the oscillatory false triggering in parallel-connected GaN-FETs. The analysis result revealed that the ratio of the common source inductance to the gate-drain capacitance of the GaN-FET should be designed within an appropriate range for preventing the oscillatory false triggering in parallel-connected GaN-FETs. Furthermore, this appropriate range was found to be slightly different from that for a single GaN-FET, which suggests that the PCB design for parallel-connected GaN-FETs needs a different parasitic inductance design instruction from that for a single GaN-FET. The appropriateness of this proposed parasitic design instruction was verified by the simulation and the experiment, suggesting the feasibility of the proposed instruction for utilizing parallel-connected GaN-FETs in high-power applications.

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