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Published in: 2017 IEEE 3rd International Future Energy Electronics Conference and ECCE Asia(IFEEC 2017 –ECCE Asia) pp.1172-1177

DOI: 10.1109/IFEEC.2017.7992207

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***Abstract*—The common source inductance is one of the major causes of deterioration of the switching speed and susceptibility of the false triggering for semiconductor switching devices. Practical design of this inductance requires selection of an appropriate semiconductor package because this inductance is greatly dependent on the physical package structure. However, few studies have reported a list of the common source inductance of commercially available packages. In order to list and compare the common source inductance among typical semiconductor packages, this paper carried out measurement of this inductance of actual switching devices mounted on experimental PCBs. This paper employed a recently proposed straightforward measurement technique directly applicable to switching devices mounted on PCBs. As a result, a basic database of the common source inductance of typical packages was presented. The common source inductance was found to be determined mainly by the package type. However, in TO-247 and TO-220 packages, approximately one-third of the total common source inductance was found to possibly vary among the switching devices of the same package due to the dependence on the current rating. Investigation of the physical package structure implied that this dependence was caused by the stray inductance of the bonding wires connecting the semiconductor chip to the source terminal.**

Keywords—bonding wire; common source inductance; semiconductor package; stray inductance

I. INTRODUCTION

Recent progress of the semiconductor technology has given rise to the fast switching semiconductor devices. Owing to their fast switching capability, the power converters are often operated at a high switching frequency for effective miniaturization of passive components, such as magnetic devices and capacitors. However, the fast switching may generate significant switching noise on the gate signal, thus deteriorating the switching speed or causing the false triggering of the switching device.

As pointed out in preceding studies [1]–[11], the stray inductance of the source terminal of the semiconductor package is one of the major causes of deterioration of the switching speed and susceptibility of the false triggering. Hereafter, we refer to this inductance as the common source inductance. At the switching, sudden change occurs in the source current. This change induces instantaneous noise voltage across the common source inductance, fluctuating the voltage level of the source on the semiconductor chip. As a result, this noise voltage overlaps with the gate signal. The noise voltage may lower the gate voltage at the switching transition, thus deteriorating the switching speed [1]–[9]. Furthermore, the noise voltage may induce parasitic LC oscillations in the gating circuit [10][11], thus causing the false triggering.

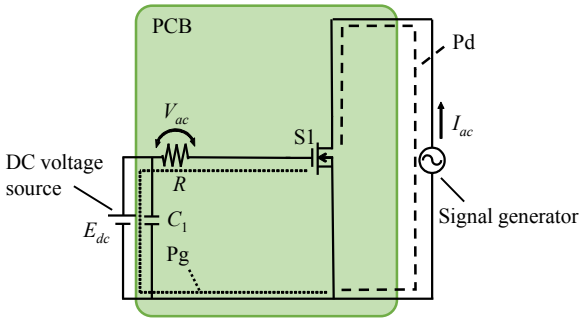
This mechanism suggests that extremely fast switching requires reduction in the common source inductance. Because this inductance is intensely dependent on the structure of the semiconductor package [1][6][11], selecting a switching device in an appropriate package with minimum common source inductance may be essential for designing fast switching power converters. However, manufactures of the switching devices generally provide no data on the stray inductance of the packages including the common source inductance. Moreover, few studies have reported quantitative comparison of this inductance among typical packages.

The reason may lie in the following two difficulties in measuring the common source inductance. Firstly, this inductance is generally too small to be measured conveniently by normal impedance measurement methods using the impedance analyzers or the network analyzers. Secondly, measurement of this inductance generally needs to determine the voltage level of the source on the semiconductor chip, as exemplified in [12], although the semiconductor chip is hidden beneath the mold and direct measurement of this voltage level is not convenient for many electronic engineers.

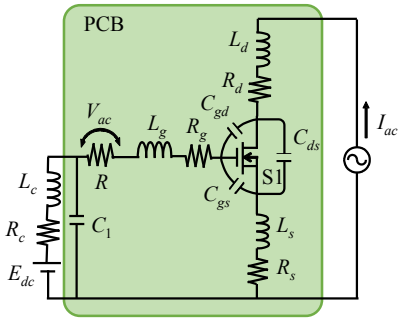
Certainly, a number of studies utilize the FEM analysis to estimate the common source inductance [2], [8], [13]–[19]. However, the FEM analysis needs detailed knowledge of the internal structure of the semiconductor package, which is generally hidden beneath the mold. Furthermore, measurement based on an experiment should be more preferable than the estimation based on simulation.

To cast a new light on this issue, [20] has recently proposed a promising measurement technique of the common source inductance, as reviewed in the next section. This technique can directly measure the common source inductance without removing the mold of the package. In addition, this technique is directly applicable to a switching device mounted on a PCB.

This work was supported by JSPS KAKENHI Grant Number JP16K06223.



(a) Circuit diagram



(b) Equivalent circuit model

Fig. 1. Circuit diagram and equivalent circuit model of the common source inductance measurement method.

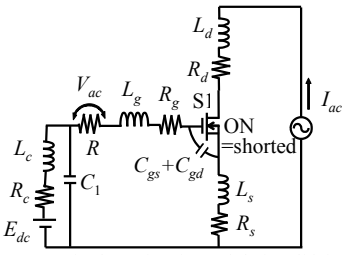
Besides, this technique is convenient because it needs common instruments for electric engineers. Actually, this technique needs only a sinusoidal signal generator and an oscilloscope.

The purpose of this paper is to list and compare the common source inductance among typical commercially available packages to provide a basic database for practical design of fast switching power converters. Based on this recently proposed measurement technique, this paper measured the common source inductance of actual semiconductor switching devices mounted on experimental PCBs. The next section presents a brief review of this measurement method. Then, section 3 presents the experiment. Finally, section 4 gives the conclusions.

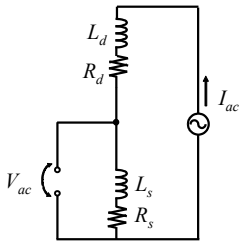
II. Measurement of the Common Source Inductance

Figure 1(a) illustrates the circuit diagram that explains the measurement method employed in this paper. Semiconductor switch S1 is the device under test mounted on a PCB. The drain and source terminals are connected to the signal generator to supply the sinusoidal AC current to the drain. Resistor R and smoothing capacitor C_1 is attached on the PCB to connect the gate and source terminals of S1. Capacitor C_1 is supplied with the DC voltage E_{dc} by the DC voltage source. Voltage E_{dc} is set at a voltage that suffices to keep S1 at the on-state. Then, the current from the signal generator and the voltage across R is measured using an oscilloscope.

In order to discuss the measurement principle, we express the circuit diagram Fig. 1(a) as the equivalent circuit model that incorporates the stray capacitance of S1 as well as the stray inductance and resistance of the wiring. Figure 1(b) illustrates the equivalent circuit model. Capacitance C_{gs}, C_{gd}, and C_{ds} are the stray capacitance of S1 between the gate and the source,



(a) Equivalent circuit model simplifying the stray capacitance of S1



(b) Final equivalent circuit

Fig. 2. Simplified equivalent circuit models based on Fig. 1(b).

between the gate and the drain, and between the drain and the source, respectively. Inductance L_g and L_d are the stray inductance of wire path Pg, i.e. the wire path that connects the gate and source terminals of S1 via R and C_1 (marked by the dotted line), and wire path Pd, i.e. the wire path that connect the drain and source terminals of S1 via the signal generator (marked by the dashed line), respectively. Resistance R_g and R_d are the stray resistance of Pg and Pd, respectively. Inductance L_c and resistance R_c are the stray inductance and resistance of the cable that connect the DC voltage source to C_1. In addition, L_s and R_s are the common source inductance and the common source resistance.

The measurement method requires C_1 and R to satisfy the following two requirements. One is that C_1 should have far larger capacitance than C_{gs}. The other is that R should have sufficiently larger resistance than the impedance of C_{gs}, L_g, and L_s at the frequency of the AC current supplied by the signal generator.

Because the DC voltage E_{dc} is applied to the gate of S1, S1 is kept at the on-state. Hence, the drain and source of the semiconductor chip can be regarded as short-circuited. This indicates that C_{ds} vanishes and C_{gd} is connected to C_{gs} in parallel. As a result, we obtain the equivalent circuit of this measurement system as Fig. 2(a).

We can further simplify the equivalent circuit, if we only consider the AC voltage and current in Fig. 2(a). Then, we can approximate that L_g, C_{gs}+C_{gd}, and C_1 are short-circuited, because they have far smaller impedance than R. Furthermore, R can be regarded as open because R generally has far larger impedance than the common source inductance and the common source resistance. As a result, Fig. 2(a) can be further expressed as a simplified equivalent circuit shown in Fig. 2(b).

As can be seen in Fig. 2(b), the measured voltage across R equals to the voltage induced in L_s and R_s. Therefore, the impedance of L_s and R_s is expressed as follows, if we denote the amplitude of the AC component of the measured voltage across

TABLE I. SEMICONDUCTOR SWITCHING DEVICES UNDER TEST.

Package	Part Number	Manufacture	DC current rating [A]	DC voltage rating [V]	Measured common source inductance [nH]	Bonding Wires		
						Number	Diameter [mm]	Length [mm]
TO-247	FQH8N100C	Fairchild	8	1000	7.4	1	0.40	6.8
	STW10NK80Z	STMicroelectronics	9	800	7.8	1	0.37	7.0
	TK28N65W,S1F(S	Toshiba	27.6	650	5.5	2	0.55	7.7
TO-220	IRFIZ34NPBF	Infineon	21	55	5.7	1	0.41	6.3
	TK32E12N1,S1X(S	Toshiba	60	120	4.9	2	0.56	5.4
	FDP120N10	Fairchild	74	100	3.9	3	0.5	6.1
I-PAK	IRFU220PBF	Vishay	4.8	200	4.3	1	0.19	3.4
	RFD14N05L	Fairchild	14	50	4.3	1	0.26	3.8
	IRLU024NPBF	Infineon	17	55	3.7	1	0.31	3.6
D2-PAK	IRF624SPBF	Vishay	4.4	250	6.1	1	0.25	4.1
	IRLZ24NSPBF	Infineon	18	55	4.9	1	0.48	4.2
	FQB33N10TM	Fairchild	33	100	5.0	1	0.46	4.2
D-PAK	IRFR224PBF	Vishay	3.8	250	3.0	1	0.32	2.5
	TK10P60W,RVQ(S	Toshiba	9.7	600	2.5	1	0.56	3.4
	NTD3055L104T4G	ON Semiconductor	12	60	3.0	1	0.38	3.3
	IRFR13N20DPBF	Infineon	13	200	2.8	2	0.36	3.4
	IRLR3410PBF	Infineon	17	100	2.9	1	0.23	3.3
	IRFR024NPBF	Infineon	17	55	3.2	1	0.31	3.4
	FDD8447L	Fairchild	50	40	2.3	2	0.44	3.3
SOT-223	IRFL014PBF	Vishay	2.7	60	2.6	—	—	—
	IRLL2703PBF	Infineon	5.5	30	2.3	—	—	—
	FDT459N	Fairchild	6.5	30	2.3	—	—	—
SOT-23	2N7002ET1G	ON Semiconductor	0.26	60	1.4	—	—	—
	FDN359AN	Fairchild	2.7	30	1.4	—	—	—
	IRLML2502PBF	Infineon	4.2	20	1.6	—	—	—

R and the measured current from the signal generator as V_{ac} and I_{ac}, respectively:

$$R_s + j\omega L_s = \frac{V_{ac}}{I_{ac}}\left(\cos\phi + j\sin\phi\right), \tag{1}$$

where ω is the angular frequency of the AC current, and ϕ is the phase difference between the measured voltage and current. Therefore, L_s can be determined as

$$L_s = \frac{V_{ac}}{\omega I_{ac}}\sin\phi\,. \tag{2}$$

As we have seen above, this measurement method has the three attractive features. Firstly, this method does not need to remove the mold of the package. Secondly, this method is applicable to a switching device mounted on a PCB. Thirdly, this method can be implemented by a straightforward measurement system with common instruments for electric engineers, such as a signal generator and an oscilloscope.

III. EXPERIMENT

Experiment was carried out to evaluate the common source inductance of typical semiconductor packages mounted on double-sided PCBs. The tested packages, as well as the experimental semiconductor devices representing these packages, are listed in Table I. Photographs of these packages are shown in Fig. 3. These packages were mounted on experimental PCBs. Specifications of the common source inductance measurement system is presented in Table II.

Figure 4 shows the experimental PCB employed for the measurement of TO-247 package. Because inappropriate layout of a PCB may add common source inductance, as shown later, all of the experimental PCBs were designed to minimize this additional common source inductance. For this purpose, the experimental PCBs satisfied the following three features in the layout pattern:

1. Wire paths Pd and Pg were designed to share no current path on the PCB except for the one point directly connected to the source terminal of the package.

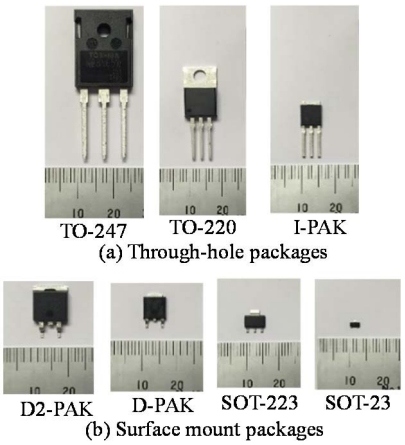


Fig. 3. Photographs of the semiconductor packages under test.

TABLE II. SPECIFICATIONS ON THE MEASUREMENT SYSTEM

Item	Value
R	1MΩ
C_1	0.15μF
E_{dc}	12V
Frequency of I_{ac}	7–11MHz
Amplitude of I_{ac}	0.1A

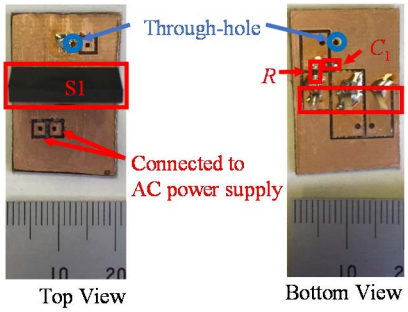


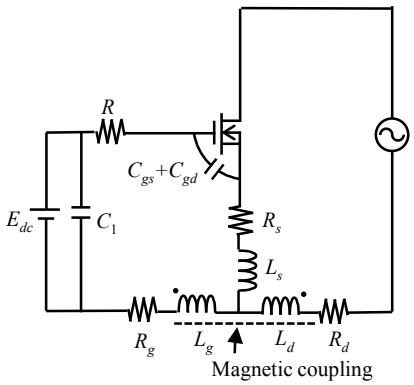
Fig. 4. Photographs of the experimental PCB for TO-247 package.

2. Wire paths Pd and Pg were designed to avoid overlap each other.
3. The PCBs were designed to have the ground plane that covers Pd and Pg.

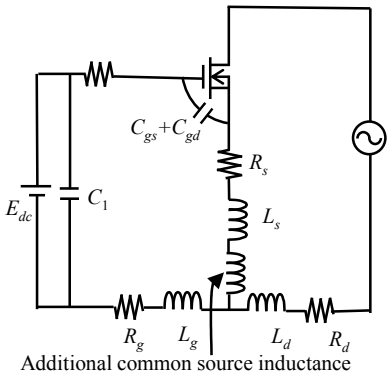
The second and third features are important to avoid undesired magnetic coupling between Pd and Pg.

The magnetic coupling between Pd and Pg is equivalent to the additional common source inductance. Below, we explain the reason based on the equivalent circuit model presented in Fig. 2(a).

The magnetic coupling between Pd and Pg appears as the parasitic transformer. Therefore, the equivalent circuit of the measurement system can be expressed as Fig. 5(a). This parasitic transformer can be equivalently replaced by a T-shaped connection of inductors, resulting in Fig. 5(b). The result indicates that the mutual inductance of Pd and Pg works as the undesired additional common source inductance, which should



(a) Equivalent circuit model with a parasitic transformer



(b) Simplified equivalent circuit model of Fig. 5(a)

Fig. 5. Modified equivalent circuits of Fig. 2(a) considering the magnetic coupling between wire paths Pg and Pd.

be minimized for evaluation of the common source inductance contributed by the packages.

Table I lists the measurement results of the common source inductance; and Fig. 6 presents comparison among typical packages. The horizontal axis in Fig. 6 is the DC current rating of the switching devices to investigate the dependence on the current rating.

Figure 6(a) shows the result of the through-hole packages. The common source inductance ranged from 3nH to 8nH. This inductance was found to be dominantly determined by the package type. Smaller package such as I-PAK showed less common source inductance as is naturally supposed. However, TO-247 and TO-220 packages showed comparatively large variety among the devices of the same package. Actually, one-third of the total common source inductance was found to vary due to the dependence on the current rating.

As for the surface mount packages, the common source inductance ranged from 1nH to 6nH. This inductance was also found to be dominantly determined by the package type. However, no apparent dependence on the current rating was found in the surface mount packages.

To summarize, the common source inductance was found to be mainly determined by the package types. However, TO-247 and TO-220 packages further showed additional dependence on the current rating. In the next section, the reason of this

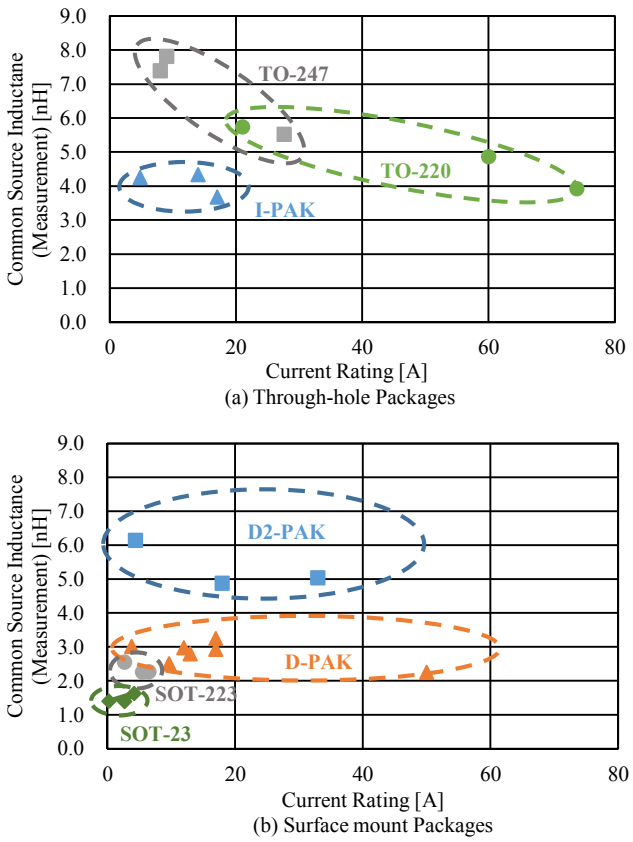


Fig. 6. Measurement results of the common source inductance.

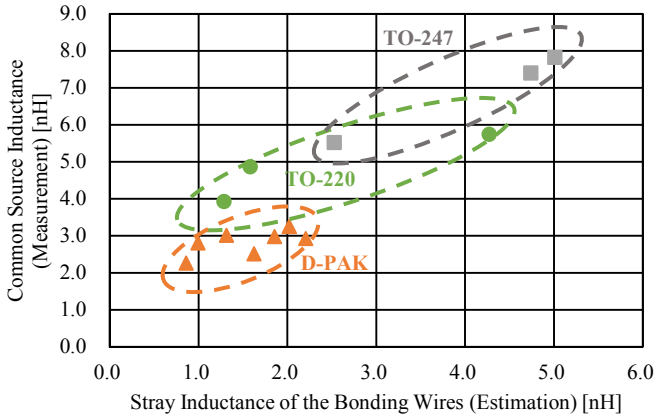


Fig. 7. Comparison of the stray inductance of the bonding wires with the measured common source inductance

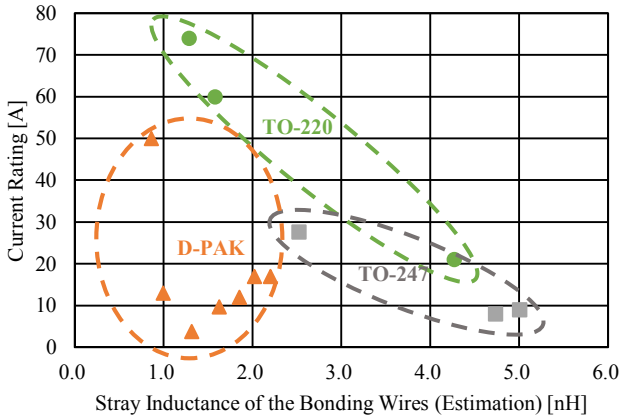


Fig. 8. Comparison of the stray inductance of the bonding wires with the current rating.

dependence is investigated by analyzing the physical structure of the package beneath the mold.

IV. Dependence on the Current Rating

This section investigates the physical package structure beneath the mold to elucidate the reason of the dependence on the current rating among the switching devices of TO-247 and TO-220 packages. Generally, a semiconductor chip is directly mounted on a base plate, which forms the drain terminal. Therefore, the stray inductance of the drain terminal may have little variety among the switching devices of the same package. On the other hand, the semiconductor chip is connected to the source terminal through the thin bonding wires. Particularly, the bonding wires tend to have large variety in the diameter, the length, and the number. As a result, the common source inductance may have comparatively large variety among the switching devices even of the same package. Therefore, we investigated the dependence of the common source inductance on the bonding wires.

No data on the bonding wires generally appear in the datasheets provided by the manufacturers of the switching devices. Therefore, we observed the bonding wires hidden beneath the mold by removing the mold mechanically using a handy grinder. Then, we measured the diameter, the length, and the number of the bonding wires that connect the semiconductor chip to the source terminal. The results is summarized in Table I. (As for SOT-223 and SOT-23, we failed to expose the bonding wires because of too small package size. Therefore, no parameters of the bonding wires were obtained for these packages.)

According to the electromagnetism, a round thin wire with the diameter r and the length l has the stray inductance L_{wire} expressed as [21]

$$L_{wire} = \frac{\mu_0 l}{2\pi}\left(\ln\frac{4l}{r} - \frac{3}{4}\right), \tag{3}$$

where μ_0 is the permeability of the vacuum. Therefore, we can estimate the common source inductance contributed by the wire bonding L_{bw} as

$$L_{bw} = \frac{\mu_0 l}{2\pi N}\left(\ln\frac{4l}{r} - \frac{3}{4}\right), \tag{4}$$

where N is the number of the bonding wires connected in parallel. We calculated L_{bw} based on (4); and compared the result with the common source inductance measured in section III as well as the current rating of the switching devices. However, SOT-223 and SOT-23 are omitted from the comparison because no data of the bonding wires were obtained. In addition, I-PAK and D2-PAK are also omitted because difference in L_{wb} was

found to be too subtle among the tested devices to discuss the dependence.

Figure 7 shows the comparison result with the measured common source inductance. As can be seen in the figure, the stray inductance of the bonding wires was found to have close correlation with the common source inductance in TO-247 and TO-220 packages. The similar relation was also found in D-PAK package, although the correlation was weak.

Figure 8 shows the comparison result with the current rating. The result revealed that stray inductance of the bonding wires have comparatively good correlation with the current rating in TO-247 and TO-220 packages, whereas no apparent correlation was found in D-PAK package. This result implies that the bonding wires is the main reason of the dependence of the common source inductance on the current rating in TO-247 and TO-220 packages.

V. CONCLUSIONS

The common source inductance is one of the major causes of deterioration for the switching speed and susceptibility of the false triggering of semiconductor switching devices. Therefore, reducing the common source inductance is intensely required for fast switching. Selecting an appropriate semiconductor package with minimum common source inductance may be essential for designing fast switching power converters because the physical structure of the package significantly contributes to the common source inductance.

In order to list and compare the common source inductance of typical commercially available packages, this paper carried out measurement of this inductance in actual switching devices mounted on PCBs. As a result, a basic database of the common source inductance of typical packages was presented. The common source inductance was found to have dominant dependence on the package type. In addition, dependence on the current rating was found in TO-247 and TO-220 packages. Investigation of the physical package structure implied that this dependence is caused by the stray inductance of the bonding wires, which tends to have correlation with the current rating.

REFERENCES

[1] T. Hashimoto, M. Shiraishi, N. Akiyama, T. kawashima, T. Uno and N. Matsuura, "System in package (SiP) with reduced parasitic inductance for future voltage regulator," IEEE Ind. Power Electron., vol. 24, no. 6, pp. 1547–1553, Jun. 2009.

[2] Y. Xiao, H. Shah, T. P. Chow and R. J. Gutmann, "Analytical modeling and experimental evaluation of interconnect parasitic inductance on MOSFET switching characteristics," in Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC2004), vol. 1, pp. 516–521, Feb. 2004.

[3] Z. Chen, D. Boroyevich and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in Proc. Intl. Power Electron. Conf. (IPEC2010), pp. 164–169, Jun. 2010.

[4] A. Gaito, R. Scollo, G. Panebianco and A. Raciti, "Impact of the source-path parasitic inductance on the MOSFET commutations," in Proc. Energy Conversion Congr. Expo. (ECCE2012), pp. 1367–1373, Sept. 2012.

[5] Bo Wang, R. Chen and D. Jauregui, "Common source inductance (CSI) of power devices and the impacts on synchronous buck converters," in Proc. Appl. Power Electron. Conf. Expo. (APEC2014), pp. 157–162, Mar. 2014.

[6] C.G. Stella, M. Laudani, A. Gaito and M. Nania, "Advantage of the use of an added driver source lead in discrete power MOSFETs," in Proc. Appl. Power Electron. Conf. Expo. (APEC2014), pp. 2574–2581, Mar. 2014.

[7] H. Li and S. Munk-Nielsen, "Detail study of SiC MOSFET switching characteristics," in Proc. IEEE Intl. Sympo. Power Electron. Distributed Generation Syst. (PEDG2014), pp. 1–6, Jun. 2014.

[8] Z. Wang, J. Zhang, X. Wu and K. Sheng, "Analysis of stray inductance's influence on SiC MOSFET switching performance," in Proc. Energy Conversion Congr. Expo. (ECCE2014), pp. 2838–2843, Sept. 2014.

[9] P. Nayak, M. V. Krishna, K. Vasudevakrishna and K. Hatua, "Study of the effects of parasitic inductances and device capacitances on 1200V, 35A SiC MOSFET based voltage source inverter design," in Proc. IEEE Intl. Conf. Power Electron. Drives Energy Syst. (PEDES2014), pp. 1–6, Dec. 2014.

[10] J. Wang and H. S.-H. Chung, "Impact of parasitic elements on the spurious triggering pulse in synchronous buck converter," IEEE Trans. Power Electron., vol. 29, no. 12, pp. 6672–6685, Dec. 2014.

[11] S. Guo, L. Zhang, Y. Lei, X. Li, W. Yu, and A. Q. Huang, "Design and application of a 1200V ultra-fast integrated silicon carbide MOSFET module," in Proc. IEEE Appl. Power Electron. Conf. Expo., 2016, May, pp. 2063–2070.

[12] On Semiconductor, "Methods to characterize parasitic inductance and resistance of modern VRM," Rep. no. AND9410/D, Apr. 2016. [Online] Available: http://www.onsemi.jp/pub_link/Collateral/AND9410-D.PDF

[13] R. Azar, F. Udrea, W. T. Ng, F. Dawson and F. Findlay, "The current sharing optimization of paralleled IGBTs in a power module title using a PSpice frequency dependent impedance model," IEEE Trans. Power Electron., vol. 23, no. 1, pp. 206–217, Jan. 2008.

[14] S. Li, L. M. Tolbert, F. Wang and F. Z. Peng, "Reduction of stray inductance in power electronic module using basic switching cells," in Proc. IEEE Energy Conversion Congr. Expo. (ECCE2010), pp. 2686–2691, Sept. 2010.

[15] B. Witting, O. Muehlfeld and F. W. Fuchs, "Adaption of MOSFETs current slope by systematic adjustment of common source stray inductance and gate resistance," in Proc. European Conf. Power Electron. Appl. (EPE2011), pp. 1–10, Aug. 2011.

[16] L. Popova, R. Juntunen, T. Musikka and M. Lohtander, "Stray inductance estimation with detailed model of the IGBT module," in Proc. European Conf. Power Electron. Appl. (EPE2013), pp. 1–8, Sept. 2013.

[17] R. Fu, A. Grekov, K. Peng and E. Santi, "Parasitic modeling for accurate inductive switching simulation of converters using SiC devices," in Proc. Energy Conversion Congr. Expo. (ECCE2013), pp. 1259–1265, Sept. 2013.

[18] Z. Liu, X. Huang and F. C. Lee, "Package parasitic inductance extraction and simulation model development for the high-voltage cascade GaN-HEMT," IEEE Trans. Power Electron., vol. 29, no. 4, Apr. 2014.

[19] Z. Miao, Y. Mao, K. Ngo and W. Kim, "Package influence on the simulated performance of 1.2kV SiC modules," in Proc. IEEE Wide Bandgap Power Devices Appl. (WiPDA2015), pp. 306–311, Nov. 2015.

[20] K. Aikawa, K. Umetani, and E. Hiraki, "A measurement method of parasitic source inductance for MOSFET mounted on the PCB," in Proc. IEEJ Ind. Appl. Soc. Conf., Maebashi, Japan, 2016, vol. 1, pp. 209–212. (in Japanese)

[21] F. W. Grover, "Parallel elements of equal length," in *Inductance calculations*, Mineola, NY, USA: Dover, 2009, pp. 31–44.