Non-isolated Interleaved High Step-down DC-DC Converter with Reduced Switched Capacitor Stages and Automatic Current Sharing

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***Abstract*—A high-voltage dc power supply system is an attractive solution for reducing the system cost and improving efficiency. This system needs compact but high-efficiency high-step-down converters to exploit the benefits. This paper proposes a novel converter for a better candidate than traditional converters. The proposed converter is a non-isolated high step-down converter utilizing the switched capacitor technology. Compared to conventional similar topologies, the number of switched capacitor stages can be reduced, enabling the compact converter design. Furthermore, this converter has interleaved output, which can downsize the magnetic devices. The current of the interleaved output is automatically balanced without special control, enabling simple controller implementation. These features were successfully verified by the experiment.**

Keywords—dc-dc converter, high step-down converter, non-isolated topology, Switched capacitor.

I. INTRODUCTION

The recent rapid and global widespread of information and communication technologies imposes an increasing burden on the information infrastructure [1]. As a result, the data centers consume increasingly large electric power, requesting a more compact and higher efficiency power supply system to cope with increasing power demand under restrictions of limited installation space and cooling capacity. The high-voltage dc power (HVDC) system is a promising technology to solve this problem [2]–[4].

Compared to the conventional ac-based power supply system, the HVDC system supplies the high-voltage dc power directly to the servers, as depicted in Fig. 1. The HVDC system can reduce the system installation space and improve efficiency by eliminating unnecessary the ac-dc and dc-ac conversion stages. Additionally, the high-voltage power line can utilize the thinner wires, which also contributes to reducing the installation space.

Despite the attractive feature, however, the HVDC system needs high step-down dc-dc conversion to interface the HVDC power supply line to the low-voltage power line for the point-of-load (PoL) converters, which finally generates the stable dc power and feeds it to the server's internal chips like processors and memory ICs. The typical step-down dc-dc converters, like buck choppers, can operate with a limited step-down ratio between the input and output voltages. Therefore, the high step-down dc-dc conversion has been achieved by a series-connection of step-down dc-dc converters. In fact, many current HVDC systems interface dc power with hundreds of volts to the conventional 12V or 48V dc bus. Then, this 12V or 48V dc power is further converted into much smaller voltages for the dc power supply suitable for the PoL converters. However, these multiple consecutive processes for step-down conversion can hinder exploiting the benefits of the HVDC system in compactness and high efficiency.

To solve this problem, many high step-down converter topologies have been proposed. Some of these converters utilize the transformer (or coupled inductor) to achieve a high step-down ratio [5]-[9]. The transformer of these topologies is commonly made of MnZn ferrite because high magnetizing inductance is important for achieving high efficiency. However, MnZn ferrite can hardly accept high frequency operation at more than 1MHz. This limit of the operating frequency can hinder the converter miniaturization.

To avoid this operating frequency limitation, other converters [10]–[13] adopt transformer-less topologies. Because they are free from transformers, these converters can operate at higher frequencies than transformer-based converters. Nonetheless, these transformer-less converters

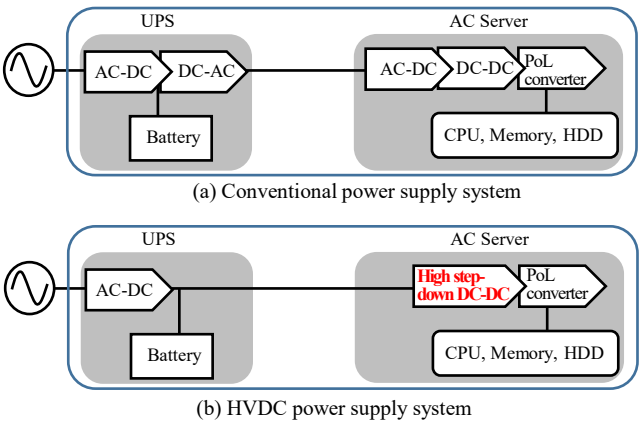

Fig. 1. Typical power supply system structures for data centers.

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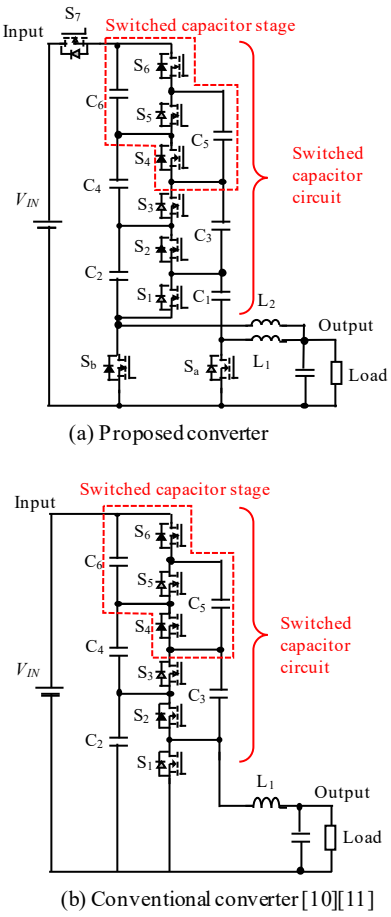

Fig. 2. Proposed and conventional non-isolated high step-down converters with 3 switched capacitor stages.

tend to suffer from large numbers of circuit elements because many of them need to have a voltage multiplier with multiple stages to achieve a low output voltage. Consequently, the transformer-less converters can also find difficulty in converter miniaturization.

The solution may lie in a transformer-less step-down dc-dc converter that can achieve a high step-down ratio with a small number of voltage multiplier stages. The purpose of this paper is to propose such a novel high step-down converter. The proposed converter can be regarded as an improved circuit based on an already-proposed converter [14] to enable a higher step-down ratio by further incorporating a voltage multiplier. At the same time, among the existing transformer-less converters with a voltage multiplier, the proposed converter can also be regarded as an improved circuit based on that proposed in [10][11]. Compared to [10][11], this converter can reduce the number of voltage multiplier stages, which results in reducing the total number of circuit elements for implementing an extremely high step-down ratio, as discussed in this paper.

In addition to these attractive features for miniaturization, the proposed converter has an interleaved output, which can reduce the output current ripple and therefore contributes to reducing the total inductor size for the output current smoothing. Certainly, typical converters with interleaved output [15]–[17] suffer from implementing a special control to balance the current of two output inductors, which will increase the controller circuit size for current sensing and feedback control. However, as discussed in this paper, the proposed converter can automatically balance the inductor current without control, enabling a simple controller implementation.

II. Proposed Converter

A. Circuit Topology

Figure 2(a) illustrates the proposed converter. The proposed converter comprises a switched capacitor circuit, which work as the voltage multiplier, two inductors L1 and L2, and two switches Sa and Sb. The proposed converter is similar to an already-proposed converter [10][11], shown in Fig. 2(b). However, the proposed converter adds Sa, Sb, S7, L2, and C1 to form the interleaved output. As discussed later, this can significantly improve the step-down performance.

B. Operating Principles

The proposed converter operates switches Sa and Sb with the 180-degree phase shift to achieve the interleaved operation. Switches S1, S3, … operate complementarily to Sb, whereas switches S2, S4, … operate complementarily to Sa. Additionally, the proposed converter does not accept the moment during which both Sa and Sb are in the off-state. Therefore, the sum of the duty cycles of Sa and Sb must be greater than 1.

Consequently, the operation comprises 3 modes. In mode 1, switches S1, S3, … are in the on-state, while Sa is in the on-state and Sb in the off-state. In mode 2, both switches S1, S3, … and switches S2, S4, … are in the off-state, while Sa and Sb are both in the on-state. In mode 3, switches S2, S4, … are in the on-state, while Sa is in the off-state and Sb is in the on-state. Figures 3 and 4 show the operating waveforms and current patterns of these operating modes.

In mode 1, switch S7 is in the on-state. Therefore, the input current flows through capacitors C2, C4, …, charging these capacitors, and finally flows out from the output terminal through inductor L2. At the same time, switches S1, S3, … are in the on-state, and therefore capacitors C1, C3, … discharge their charge to the output terminal, while simultaneously charging capacitors C2, C4, …. During this discharging process, inductor L2 is applied with the positive voltage that increases the output current. (The inductor voltage is defined as subtraction of the voltage potential at the inductor terminal connected to the output from that at the other inductor terminal.) Meanwhile, the current of inductor L1 also continues to flow through the output terminal due to its inductance. However, as Sa is in the on-state, L1 is applied with the negative voltage that decreases the output current linearly.

In mode 2, only switches Sa and Sb are in the on-state. Therefore, no current flows through the input terminal. Additionally, both capacitors C1, C3, … and capacitors C2, C4, … can be neither charged nor discharged, keeping their voltage constant. Meanwhile, inductors L1 and L2 are applied with the negative voltage to decrease the output current linearly.

In mode 3, switch S7 is in the off-state. Therefore, no current again flows through the input terminal. However, capacitors C2, C4, … can discharge their charge through switches S2, S4, … finally to the output terminal, while charging capacitors C1, C3, …. During these discharging process, inductor L1 is applied with the positive voltage that increases the output current. However, as Sb is in the on-state,

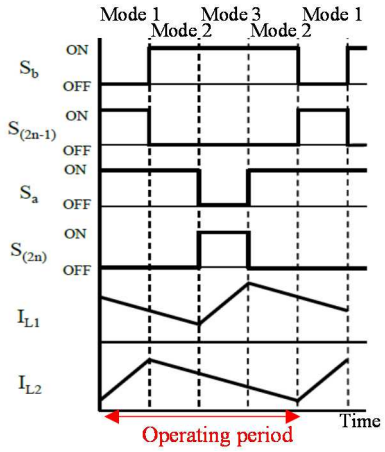

Fig. 3. Operating waveforms of proposed converter.

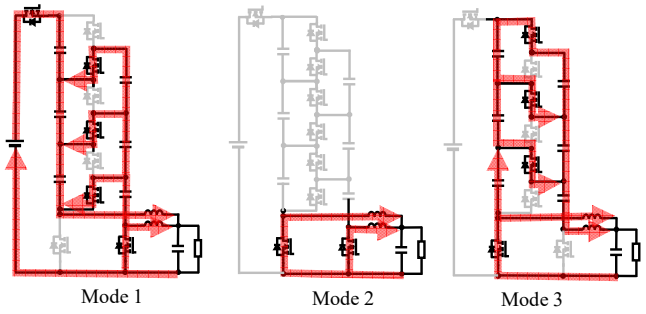

Fig. 4. Current patterns of proposed converter.

L2 is applied with the negative voltage that decreases the output current linearly.

C. Voltage Gain

The inductor voltage averaged over a whole switching period must vanish in the steady-state operation. According to the operating principle, the following voltage is applied to L1 during each mode:

$$V_{L1} = \begin{cases} V_{C2} - V_{C1} - V_{out}, & \cdots \text{mode } 3 \\ -V_{out}, & \cdots \text{mode } 1, 2 \end{cases} \tag{1}$$

where V_{C1} and V_{C2} are the voltage across C1 and C2, respectively and V_{out} is the output voltage. Similarly, the voltage applied to L2 is obtained as:

$$V_{L2} = \begin{cases} V_{C1} - V_{out}, & \cdots \text{mode } 1 \\ -V_{out}. & \cdots \text{mode } 2, 3 \end{cases} \tag{2}$$

Hence, the following relations can be obtained in the steady state operation from (1) and (2), if D_{Sa} and D_{Sb} denote the duty cycles of Sa and Sb respectively.

$$(1 - D_{Sa})(V_{C2} - V_{C1} - V_{out}) - D_{Sa}V_{out} = 0, \tag{3}$$

$$(1 - D_{Sb})(V_{C1} - V_{out}) - D_{Sb}V_{out} = 0. \tag{4}$$

According to the current patterns in Fig. 4, capacitors C2, C4, … are respectively connected in parallel with C3, C5, … in mode 1, whereas capacitors C4, C6, … are respectively connected in parallel with C3, C5, … in mode 3. Consequently, the voltage across C2, C3, C4, … must be the same as a result of repetitive parallel connection with the neighboring capacitor. Hence,

$$V_{C2} = V_{C3} = V_{C4} = \cdots. \tag{5}$$

By solving (3)-(5), the capacitor voltage in the steady-state operation is obtained as

$$V_{C1} = \frac{V_{out}}{1 - D_{Sb}}, \tag{3}$$

$$V_{C2} = \left(\frac{1}{1 - D_{Sa}} + \frac{1}{1 - D_{Sb}} \right) V_{out}. \tag{4}$$

According to the current pattern in mode 1, the input voltage must be identical to the sum of the capacitor voltage of C1, C2, C4, …. Therefore, if the number of the switched capacitor stages denotes N, the input voltage V_{in} is expressed as follows in the steady state:

$$V_{in} = V_{C1} + NV_{C2}. \tag{5}$$

(Hence, the number of capacitors in the switched capacitor is $2N$.) Consequently, the voltage gain G of the proposed converter can be obtained as

$$G = \frac{V_{out}}{V_{in}} = \frac{1}{\dfrac{N}{1 - D_{Sa}} + \dfrac{N+1}{1 - D_{Sb}}}. \tag{6}$$

If the duty cycles of S_a and S_b are identical, i.e. $D_{sa}=D_{sb}=D$, (6) can be rewritten as

$$G = \frac{V_{out}}{V_{in}} = \frac{1 - D}{2N + 1}. \tag{7}$$

Equation (7) indicates the remarkable high step-down performance with few switched capacitor stages. In fact, the conventional converter [10][11], i.e. Fig. 2(b), is reported to have a voltage gain $G=(1-D)/(N+1)$, which is approximately twice as large as that of the proposed converter if N is large. This difference in the voltage gain indicates that the proposed converter can reduce the switched capacitor stages and therefore the number of switching devices, as well as capacitors, compared with the conventional converter [10][11] designed to achieve the same step-down ratio.

D. Voltage Stress on Switches

According to Fig. 4, switches S1, S3, …, S($2N-1$) are applied in mode 3 with the voltage of capacitors C2, C4, …, C($2N$). Similarly, switches S2, S4, …, S($2N$) are applied in mode 1 with the voltage of capacitors C2, C4, …, C($2N$). (Switches S1, S2, … have equal or smaller voltage stress in mode 2 than in their off-state of mode 1 or mode 3.) Consequently, switches S1, S2, …, S($2N$) experience the voltage stress identical to V_{C2}, which is far smaller than the input voltage V_{in}.

According to the current pattern in mode 3, S($2N+1$) is applied with $V_{in}-NV_{C2}$, which is identical to V_{C1} according to

(5). Additionally, the main switches Sa and Sb are applied in their off-state with the voltage $V_{C2}-V_{C1}$ and V_{C1}, respectively. Therefore, S(2N+1), Sa, and Sb experience half the voltage stress than the other switches, if the duty cycles of Sa and Sb, i.e. D_{Sa} and D_{Sb}, are identical. It is also worth noticing that the voltage stress differs between Sa and Sb, when $D_{Sa} \neq D_{Sb}$.

E. Current Sharing Between Output Inductors

Unlike the interleaved buck chopper, the proposed converter can have different duty cycles D_{sa} and D_{sb} of the low-side switches Sa and Sb. This enables the proposed converter to be free from the current balance control between L1 and L2, which is essential for the practical control design of the interleaved buck chopper. In fact, even if $D_{sa} \neq D_{sb}$, the current ratio between L1 and L2 can be clearly determined according to the circuit theory without considering parasitic effects like parasitic resistance or the converter power loss.

As discussed in subsection II.B, capacitors C2, C4, … are charged in mode 1 and discharged in mode 3, whereas capacitors C1, C3, … are discharged in mode 1 and charged in mode 3. Let the average current flowing through S1, S3, … during mode 1 be I_{S1}, I_{S3}, … and the average current flowing through S2, S4, … during mode 3 be I_{S2}, I_{S4}, ... Noticing that the amount of charge and discharge of C1, C2, … during modes 1 and 3 must be equal in the steady state operation, the following relations can be obtained.

$$\begin{aligned}(1-D_{Sa})\sum_{n=1}^{N-k+1} I_{S(2N+2-2n)} \\ = (1-D_{Sb})\sum_{n=1}^{N-k+1} I_{S(2N+1-2n)},\end{aligned} \tag{8}$$

$$\begin{aligned}(1-D_{Sa})\sum_{n=1}^{N-k+1} I_{S(2N+2-2n)} \\ = (1-D_{Sb})\sum_{n=1}^{N-k+1} I_{S(2N+3-2n)}.\end{aligned} \tag{9}$$

Equations (8) and (9) indicate the balance between charge and discharge amount for capacitors C_{2k-1} and C_{2k}, respectively, where k is an arbitrary natural number between $1 \leq k \leq \mathrm{N}$.

Equations (8) and (9) yield the following relations:

$$(1-D_{Sa})I_{S(2k)} = (1-D_{Sb})I_{S(2k-1)}. \tag{10}$$

$$(1-D_{Sa})I_{S(2k)} = (1-D_{Sb})I_{S(2k+1)}. \tag{11}$$

Consequently, the average switching device current during their on-state has the following relation:

$$\begin{aligned}(1-D_{Sb})I_{S1} = (1-D_{Sa})I_{S2} = .(1-D_{Sb})I_{S3} \\ = (1-D_{Sa})I_{S4} = .(1-D_{Sb})I_{S5} = \cdots.\end{aligned} \tag{12}$$

On the other hand, the average current of L1 and L2 can be formulated as follows, considering that the inductor current path during mode 1 and mode 3:

$$I_{L1} = I_{S2} + I_{S4} + \cdots + I_{S(2N)}. \tag{13}$$

$$I_{L2} = I_{S1} + I_{S3} + \cdots + I_{S(2N-1)} + I_{S(2N+1)}, \tag{14}$$

where I_{L1} is the average current of L1 during mode 3 and I_{L2} is the average current of L2 during mode 1, respectively.

By utilizing (12)-(14), the relations among the switching device current I_{S1}, I_{S2}, … and the inductor current I_{L1} and I_{L2} can be obtained as

$$\frac{I_{L1}}{N} = I_{S2} = I_{S4} = \cdots = I_{S(2N)}, \tag{13}$$

$$\frac{I_{L2}}{N+1} = I_{S1} = I_{S3} = \cdots = I_{S(2N-1)} = I_{S(2N+1)}, \tag{14}$$

$$\frac{1-D_{Sa}}{N} I_{L1} = \frac{1-D_{Sb}}{N+1} I_{L2}. \tag{15}$$

Noticing that L1 increases the current throughout mode 3 and decreases it throughout modes 1 and 2, the average current of L1 during modes 1 and 2 is identical to I_{L1}. Similarly, the average current of L2 during modes 2 and 3 is also identical to I_{L2}. Hence, I_{L1} and I_{L2} can be regarded to be average inductor currents throughout the whole switching period. Therefore, (15) indicates that duty cycles D_{sa} and D_{sb} determine the current sharing between L1 and L2. In other words, the current sharing between L1 and L2 does not request accurate matching of D_{sa} and D_{sb}. The proposed converter thus does not require a special control to balance the current of two output inductors. Instead, an independent setting of D_{sa} and D_{sb} will readily result in the corresponding ratio between I_{L1} and I_{L2}.

It is worth noticing that $D_{sa} = D_{sb}$ does not result in uniform current sharing, i.e. $I_{L1}=I_{L2}$. In fact, according to (15), uniform current sharing is achieved by satisfying the following relation between the duty cycles:

$$\frac{1-D_{Sa}}{N} = \frac{1-D_{Sb}}{N+1}. \tag{16}$$

However, suppose N is designed to be large for an ultimately high step-down conversion. In that case, the straightforward duty cycle setting, i.e. $D_{sa} = D_{sb}$, can lead to acceptably good current sharing between I_{L1} and I_{L2}.

The analysis results of subsection II.C and II.D are consistent with the energy conservation of the proposed converter. In fact, the average input current I_{in} and output current I_{out} can be formulated as follows according to (13)-(15):

$$I_{in} = \frac{I_{L2}}{N+1}(1-D_{Sb}). \tag{13}$$

$$I_{out} = I_{L1} + I_{L2} = I_{L2}\left(1 + \frac{N}{1-D_{Sa}}\frac{1-D_{Sb}}{N+1}\right). \tag{14}$$

Therefore, (6), (13), and (14) yield $V_{in}I_{in}=V_{out}I_{out}$, indicating the energy conservation of the proposed converter.

TABLE I. SPECIFICATIONS OF PROTOTYPE

Input voltage (V_{in})	40V
Operating frequency	200kHz
Inductors L1, L2	10μH, 38mΩ DCR (Bourns SRR6038-100Y)
Capacitors C1-C6	4.7μF (Murata GCM32ER71H475KA55L)
MOSFET S1-S7	ZXMN6A07ZTA (DiodesZetex)
MOSFET Sa, Sb	RSD150N06TL (RohmCorp.)

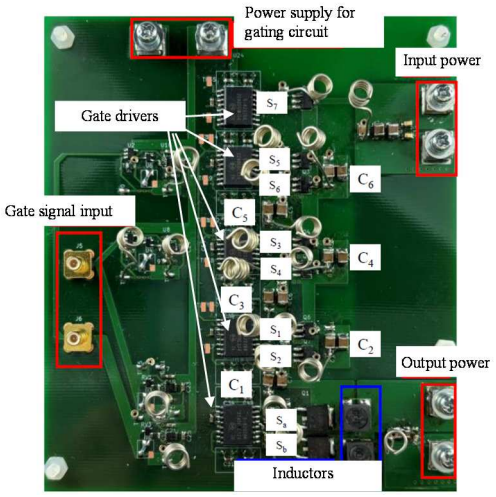

Fig. 5. Photograph of prototype of proposed high step-down converter.

F. Output Ripple Cancelation

As discussed above, inductors L1 and L2 are applied with the positive voltage during mode 3 and mode 1, respectively, and otherwise applied with the negative voltage, whose absolute value is identical to the output voltage. Therefore, because of the interleaved operation of Sa and Sb, the current ripple of inductors L1 and L2 also have a phase difference of 180 degrees. This can effectively reduce the output current ripple, enabling L1 and L2 to have a small inductance and therefore to reduce the total magnetic volume compared to the conventional high step-down converter proposed in [10][11].

III. EXPERIMENT

An experiment was carried out to verify the operating principles of the proposed converter. The prototype of the proposed converter was designed to have 3 switched capacitor stages as shown in Fig. 2(a). Table I shows the specifications of the prototype. Figure 5 shows the photograph of the prototype. The two low-side switches Sa and Sb are operated with a phase shift. A low switching frequency, i.e. 200kHz, was chosen for this experiment to easily observe the current and voltage waveforms with the oscilloscope.

A. Operating waveforms

The operating waveforms were observed when both the duty cycles D_{Sa} and D_{Sb} were set at 0.75. The output is connected with a 1Ω resistor. Then, the drain-source voltage of Sa and Sb as well as the inductor current waveforms were observed to verify the operating principles discussed in the previous section. Figure 6 shows the result. The voltage stress on Sa and Sb in their off-state was observed to be 6V approximately, which was far smaller than the input voltage. This voltage stress is consistent with the theoretical expectation, which predicted 5.7V on Sa and Sb approximately.

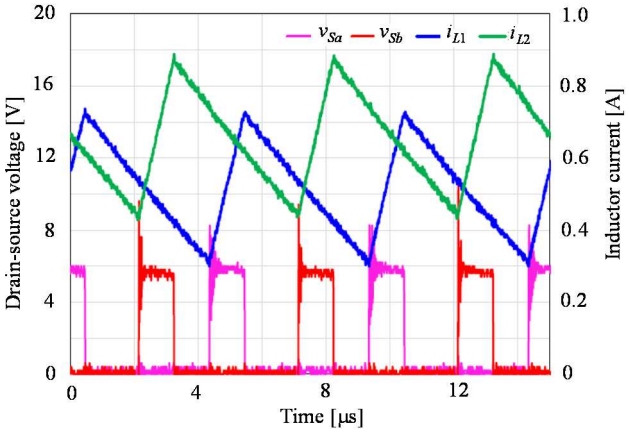

Fig. 6. Drain-source voltage waveforms (v_{Sa}, v_{sb}) of Sa and Sb and current waveforms (i_{L1}, i_{L2}) of L1 and L2 when duty cycles are set at D_{Sa}=D_{Sb}=0.75.

TABLE II. MEASUREMENT RESULT AND THEORETICAL PREDICTION OF AVERAGE CAPACITOR VOLTAGES

Capacitor	Measurement [V]	Theory [V]
C1	5.8	5.68
C2	11.16	11.37
C3	11.36	11.37
C4	11.17	11.37
C5	11.37	11.37
C6	11.17	11.37

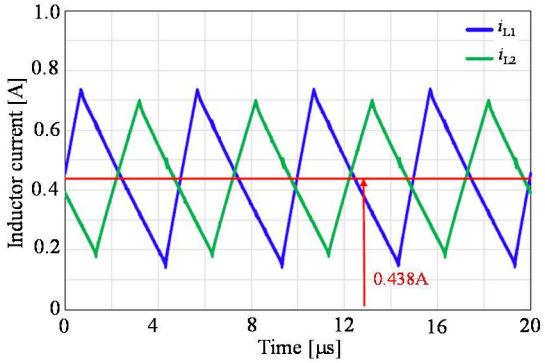

Fig. 7. Current waveforms (i_{L1}, i_{L2}) of L1 and L2 when duty cycles are set at D_{Sa}=0.7, D_{Sb}=0.6.

This reduction in the voltage stress is achieved by the switched capacitor stages. Table II shows the measurement result and the theoretical prediction of the average voltage stored in capacitors C1-C6. The measurement results agreed well with the theory, supporting the operating principles of the proposed converter.

The inductor current ripples were well interleaved between L1 and L2, which reduced the output current ripple, as expected from the theory. However, the inductor current was not well balanced. This unbalance also agrees with the theory. As seen in (15), the same duty cycles for Sa and Sb caused stable but slight unbalance between L1 and L2. This unbalance can be solved by adjusting the appropriate duty cycle difference between S1 and S2 to satisfy (16). Figure 7 shows the inductor current of L1 and L2 when the duty cycles of Sa and Sb are set at 0.7 and 0.6, respectively, after (16). The L1 and L2 currents were then adjusted to be well balanced, as is consistent with the theory.

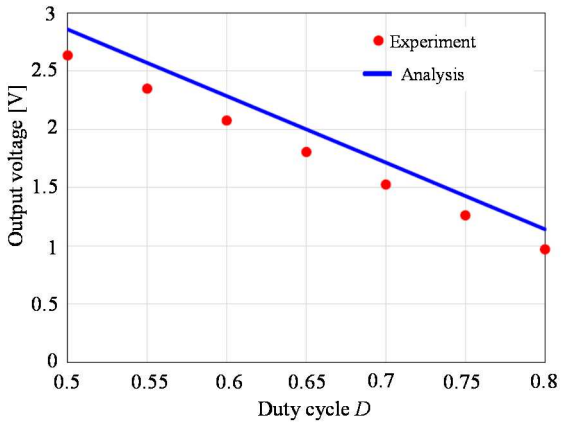

Fig. 8. Dependence of output voltage on duty cycle D. ($D = D_{Sa} = D_{Sb}$)

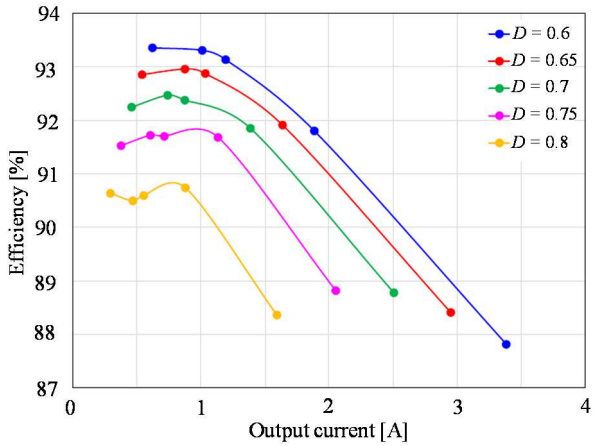

Fig. 9. Measured efficiency at various duty cycle D. ($D = D_{Sa} = D_{Sb}$)

B. Voltage Gain

Figure 8 shows the measurement result of the output voltage at various duty cycles. In this measurement, the duty cycles of Sa and Sb were set at the same value D; the load resistance was set at 3.3Ω. The result proved that the measured output voltage agreed well with the theoretical prediction calculated based on (7), which supports the promising step-down performance with a few switched capacitor stages.

C. Efficiency

Finally, the efficiency was evaluated when Sa and Sb were operated at the same duty cycle D. The result is shown in Fig. 9. The result exhibits high efficiency considering the extreme step-down ratio. The efficiency dropped as the output current increased. This is caused by the conduction loss at the switching devices. Therefore, this efficiency drop can be mitigated by optimal choice of switching devices with low on-resistance. Nonetheless, the experiment successfully verified the operating principles of the proposed converter.

IV. Conclusions

This paper proposed a non-isolated high step-down converter that outputs small dc voltage with few number of the switched capacitor stages and achieves interleaved output without any special current balancing control. Owing to these attractive features, the proposed converter is expected to be suitable for dc bus voltage converter for the HVDC power supply system of the data centers. An experiment successfully verified the operating principles of the proposed converter, elucidating its promising features for the dc bus voltage converter applications for the datacenters.

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