Vias Placement Strategy for High Power Transformers with Vertically Stacked PCBs

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***Abstract*— Isolated DC-DC converters in data centers have a high step-down ratio. This causes large high-frequency currents on the secondary side. But strong proximity effect occurs in the wires between the transformer and the rectifier. These effects cause large losses. To address this issue, an approach has been proposed to suppress proximity effect by designing the transformer windings on a PCB and directly attaching the rectifier elements to the windings. In this approach, it was assumed that PCBs would be connected in parallel in the vertical direction to compensate for the small cross-sectional area of the PCB windings. However, when connecting PCBs using vias, there is a concern that unexpected losses may occur due to proximity effects near the vias, magnetic coupling between PCBs, or other proximity effects. In this paper, after measuring the AC resistance of prototype devices with different via placements and PCB spacings, we analyze the mechanisms of loss increase using electromagnetic field analysis and provide multiple strategies for designing PCB layering.**

Keywords—Transformer, PCB, Proximity effect, Via, High Power

I. INTRODUCTION

In recent years, the development of information and communication technology has led to a steady increase in the power consumption of information and communication equipment, including data centers [1]-[3]. The power supply system of data centers supplies high DC voltage such as 400 V to reduce the current flow in cables as a result of the increase in power consumption. On the other hand, servers require low voltage such as 12 V. Therefore, isolated DC-DC converters with high step-down ratios are used. To achieve high step-down ratios, the secondary winding of the transformer is often constructed with a single turn, resulting in very large currents flowing. Especially, as shown in Fig. 1, large currents flow in opposite directions in the wires between the secondary winding and the rectifier. This causes strong

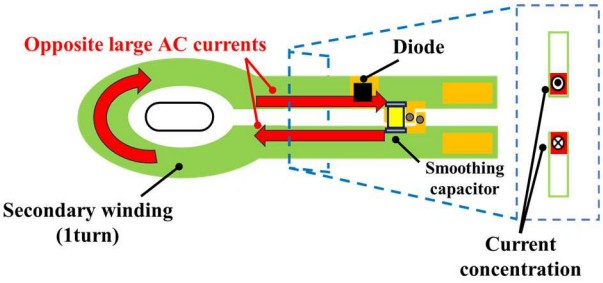


Fig. 1 Proximity effect in lead winding

proximity effect, which make the converter less efficient [4].Regarding this issue, [5] and [6] proposed the approach to suppress the proximity effect by implementing the rectifier circuit on the secondary winding directly. In this method, the transformer winding is designed on a printed circuit board (PCB). This makes it easy to mount synchronous rectification elements such as switches and gate drivers on the winding.

However, PCB windings are thin films with small cross-sectional areas, so in order to carry large currents, it is necessary to increase the cross-sectional area of the windings. There are two main approaches to increasing the cross-sectional area of windings. The first is a method of connecting PCBs horizontally and connecting the windings in parallel [7]-[11]. This method rectifies the secondary-side AC current and then combines the DC currents. So, it is not affected by proximity or skin effects. However, since the cores are arranged horizontally, the magnetic device tends to become larger in size. Furthermore, when the center tap method is applied, it has been pointed out that parasitic resonance may occur due to the inductance of the wiring connecting the smoothing capacitor and the PCB at high frequency [7]. The resonance frequency decreases as the parasitic inductance increases. Therefore, the approach of connecting PCBs horizontally may cause a particularly

significant issue, because the wiring connecting smoothing capacitors tends to become long.

The second method is to connect the PCBs vertically and configure the windings in parallel [6]. This method shares a single magnetic core and stacks PCBs, making it less likely for the magnetic device to become bulky. Additionally, even when the center tap method is applied, parasitic resonance can be suppressed by minimizing the path connecting the smoothing capacitors [6]. Furthermore, with the recent commercialization of wide bandgap semiconductors and their expected application in high-power systems [12]-[15], an approach has been proposed to improve spatial efficiency by consolidating multiple secondary-side AC currents into a single rectifying device [6]. Thus, the method of stacking PCBs vertically may be a promising approach for suppressing parasitic resonance while improving space utilization in the future as frequencies increase. However, to realize this approach, secondary-side AC currents must flow between PCBs through vias, which may result in increased losses due to skin effects and proximity effects.

Therefore, this paper aims to analyze the loss mechanisms that arise when vertically stacking multiple PCBs and to provide design strategies for PCB stacking. Experiments and simulations were conducted focusing on two main items: the proximity effect that occurs in the substrate around the via located immediately before the rectifier element, and the magnetic coupling and proximity effect between PCBs. To verify these effects experimentally, prototypes with different via placements and different PCB spacing were fabricated, and the AC resistance was measured. This paper analyzes the loss mechanisms from both experimental and simulation perspectives and provides multiple strategies for PCB stacking design.

II. Issues of Parallelization of Vertically Stacked PCBs Transformer

In this section, we discuss the issues of vertically stacked PCBs with vias, using the structure in [6] as an example. PCB makes it easy to attach components to the windings. As shown in Fig. 2, a rectifier circuit is mounted on the secondary winding, and the secondary winding and rectifier circuit are integrated to suppress the large proximity effect that occurs in the lead wires.

PCB windings have a small cross-sectional area due to their thin film structure, which limits the amount of current they can carry. Therefore, to achieve high current capacity, it is necessary to increase the cross-sectional area of the windings. In particular, since very large currents flow on the secondary side, as shown in Fig. 3(a), multiple PCBs are stacked vertically to parallelize the secondary windings. In this structure, large smoothing capacitors are mounted only on the top and bottom layers. Additionally, mounting rectifier elements on each PCB would result in a large magnetic device. Therefore, two PCBs are stacked into one stack and the rectifier elements are shared to collectively rectify the secondary-side AC current. Fig. 3(b) shows the circuit diagram.

However, there is a concern that the current around the via may cause proximity effects and increase losses. For example, as shown in Fig. 4, the secondary AC current near via 2 may cause large eddy current. Furthermore, the secondary current flowing out of the via 2 follows the current path shown in Fig. 5, so opposing current components may generate a large proximity effect. In synchronous rectification, it is necessary to implement gate drive circuits and snubber circuits to suppress surges, so there are strong restrictions on via placement. As a result, as shown in Fig. 5, vias may be arranged in a concentrated configuration. In this case, AC current may concentrate in the via, potentially increasing proximity effect. On the other hand, dispersing the vias to the left and right, as shown in Fig. 6, may suppress the concentration of AC current and reduce eddy current. Furthermore, even within a dispersed configuration, placing the vias farther away from the rectifier elements may result in a more gradual change in the current vector, potentially further suppressing eddy current.

In vertically stacked PCB transformers, changes in PCB spacing may affect magnetic coupling of windings and eddy current in Fig.4.

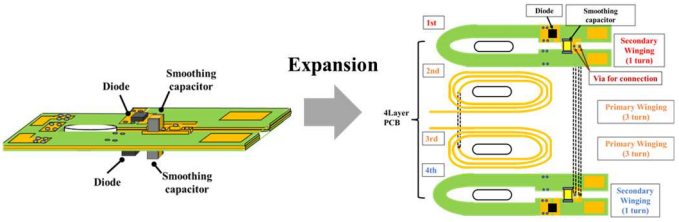
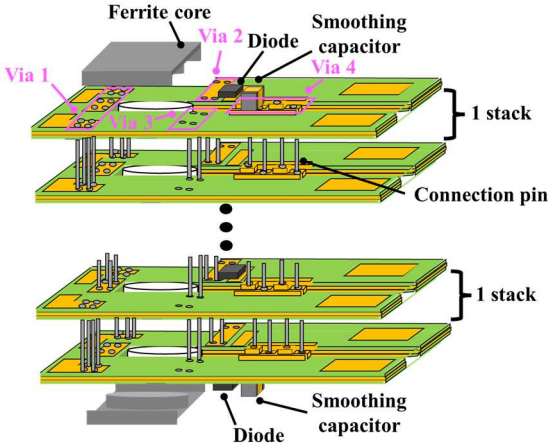
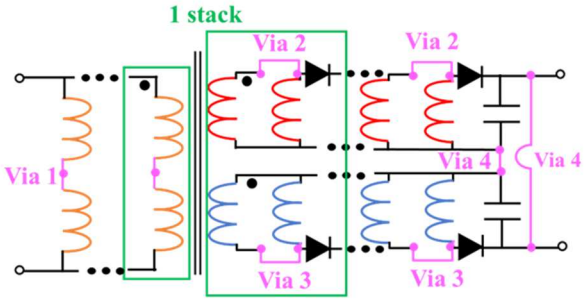


Fig. 2 PCB transformer with integrated rectifier



(a). Schematic diagram



(b). Circuit diagram

Fig. 3 Transformer with vertical stacked multiple PCBs

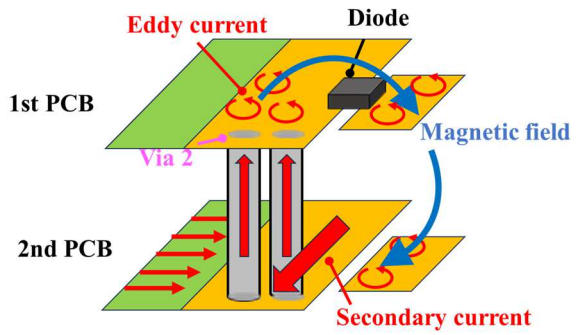


Fig. 4 Eddy current caused by secondary current near via 2

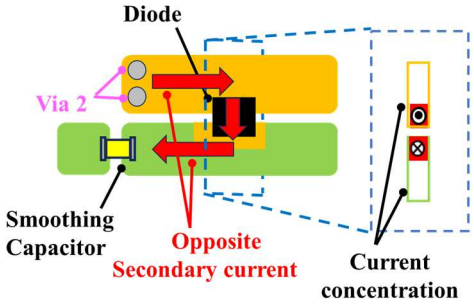


Fig. 5 Proximity effect around via 2

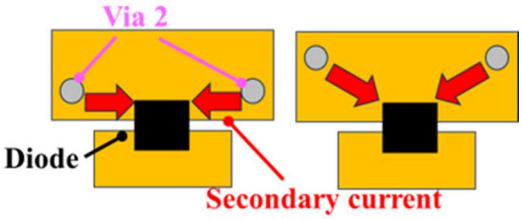


Fig. 6 Distributed placement of via 2

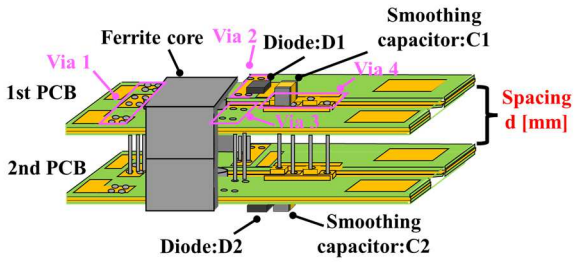
III. Vertical Stacked PCBs Transformer Under Consideration

This section explains the details of the prototype compared in the experiment and simulation.

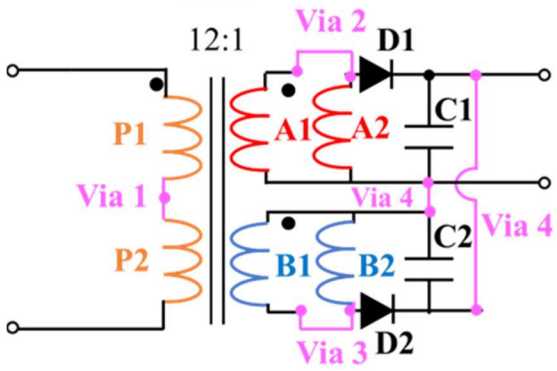
In order to avoid complicating the experiment, this study describes a structure consisting of two stacked PCBs, which is the minimum configuration required for a transformer. Fig. 7(a) shows a schematic diagram. In this structure, the rectifier circuits are also arranged on the top and bottom layers. Additionally, since the PCB spacing varies depending on the experiment, it is assumed to be d [mm]. Fig. 7(b) shows a circuit diagram. To achieve a high step-down ratio, the primary windings P1 and P2 are connected in series with 12 turns, while the secondary windings A1, A2, and B1, B2 are connected in parallel at the vias immediately before the rectifier diodes to increase the cross-sectional area. Fig.8 shows a cross-sectional view.

Fig. 9 shows a single PCB transformer before lamination. The rectifier circuit is located on the top and bottom layers. In this study, diodes (V30K202HM3/H) are used to simplify the rectifier elements, and smoothing capacitors are UMK325B7475KMHP. Additionally, this PCB transformer is composed of four layers, with 70 μm thick copper wiring. The primary winding is connected in series to increase the step-down ratio, while the secondary winding is connected in parallel to form a center tap [16]-[18] with low conduction loss. The winding width is 1.7 mm for the primary winding and 5.6 mm for the secondary winding. Fig. 10 shows the dimension of a single PCB transformer.

Fig.11 shows placements of via 2 and they were defined as placements 1 to 4, respectively. To verify the effects of proximity effect near the via 2 shown in Fig. 5, we fabricated prototypes 1 to 4 with different via 2 placements, as shown in Fig. 12. In addition, to verify the effects of magnetic coupling and eddy current near via 2, we fabricated prototypes 5 to 8, as shown in Fig. 13. Prototypes 1 to 4 and 5 to 8 differ only in PCB spacing. The PCB spacing for prototypes 1 to 4 is 0.125 mm, managed by spacers. Additionally, since the thickness of the rectifier diode (V30K202HM3/H) is 1.0 mm, the PCB spacing for prototypes 5 to 8 was designed to be 1.0 mm.



(a). Schematic diagram



(b). Circuit diagram

Fig. 7 Transformer with vertical stacked two PCBs

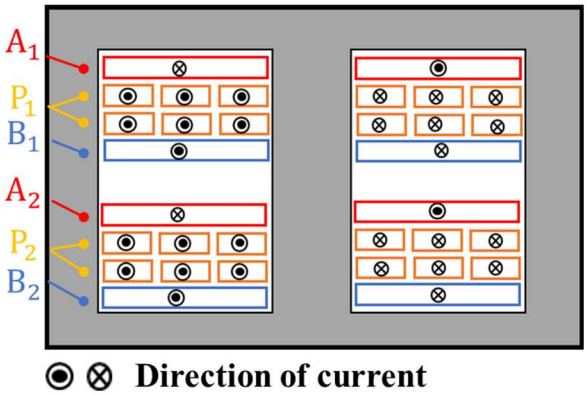


Fig. 8 Cross sectional view

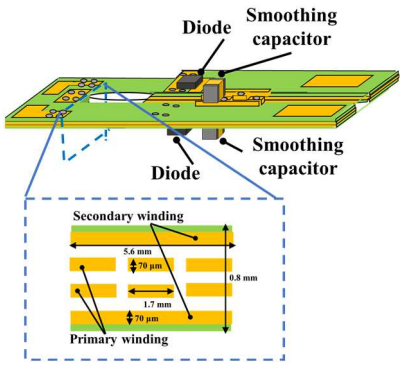


Fig. 9 Single PCB transformer

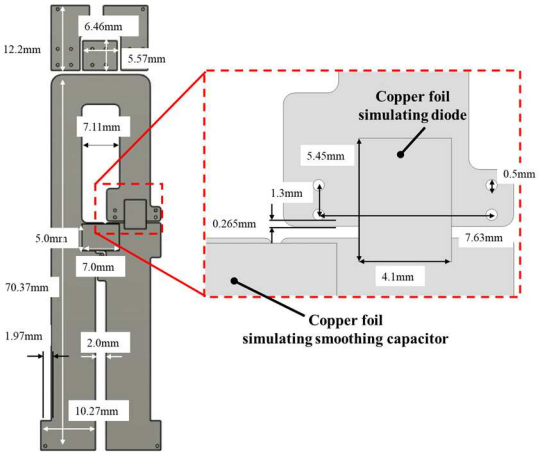


Fig. 10 Dimension of single PCB transformer

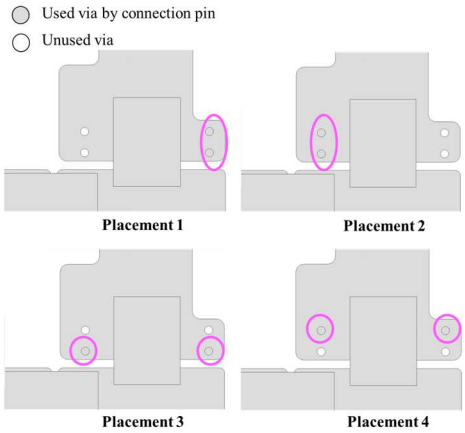


Fig. 11 Placement of via 2

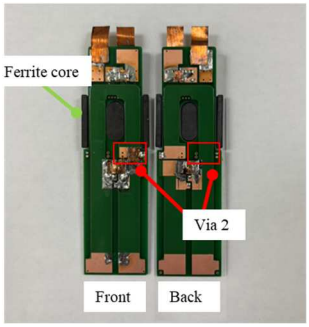


Fig. 12 Photograph of prototype 1 to 4

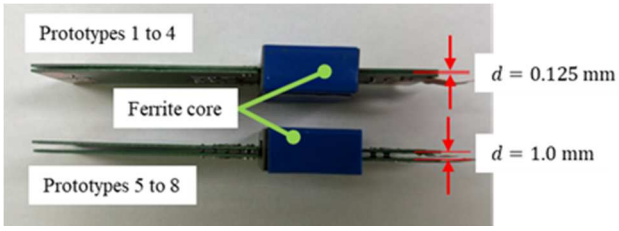


Fig. 13 Photograph of prototype 5 to 8

IV. Experiment and Electromagnetic Field Analysis of Vias Placement

In this section, we compare four prototypes 1 to 4 with different via placements through experiments and simulations.

A. Experiment

Loss is calculated as the product of AC resistance and the square of current. Therefore, evaluating AC resistance means evaluating loss. In the experiment, AC resistance of prototypes 1 to 4 was compared to verify the extent of the effect of via placements on loss. Fig.14 shows experimental circuit diagram. To reproduce the AC current path in the center-tapped transformer, diode D1, smoothing capacitors C1, and C2 are shorted using copper foil with dimensions equivalent to the component sizes. Meanwhile, diode D2 is left open. LCR meter (nf circuit diagram block ZM2376) was connected to the primary side of the prototypes. AC resistance was measured six times at 1 MHz and the average value was calculated. The two sample t-test confirmed the validity of the measurements. A two-tailed test with a significance level of 5% was performed on the measured values of prototypes 2 and 3.

Fig. 15 shows a comparison of the increase in AC resistance due to PCB lamination in each prototype. These values are calculated by subtracting the AC resistance of an ideal transformer with no connection loss from the total AC resistance of the transformer measured with LCR meter. The resistance of the ideal transformer should be half of the resistance of the single PCB transformer. But the turn ratio of the single PCB transformer is 6:1. On the other hand, that of an ideal transformer is 12:1. Thus, the following equation holds true for the resistance R_{i} of the ideal transformer and the resistance R_{s} of the single PCB transformer.

$$r = \frac{R_i}{4R_s}$$

r is the resistance ratio between R_i and $4R_s$,which is 0.5. The result measured with LCR meter was $R_{\mathrm{s}} = 251\ \mathrm{m\Omega}$. As shown in Fig. 15, even prototype 4, which has the smallest loss via placement, showed a 20% increase in loss compared to the AC resistance of the ideal transformer. This is a significant increase that cannot be ignored, suggesting the importance of discussing the losses generated by via connections. Next, we compare the AC resistance between prototypes 1 and 4. The increase in loss for prototype 1 is approximately 1.4 times that of prototype 4, indicating a significant increase in loss. Therefore, it is clear that the vias placement significantly affects the loss caused by PCB lamination.

B. Electromagnetic field analysis

In this subsection, we analyze the mechanism of loss

differences due to vias placement using electromagnetic field analysis. As shown in Fig.16, we created analysis models of prototypes 1 to 4 using JMAG and applied 1Arms sinusoidal current to the primary winding. For simplicity of analysis, the model of wiring through which no current flows was omitted.

Fig. 17 shows the breakdown of losses for each layer of prototypes 1 to 4. As expected, the first layer, which has a rectifier circuit, showed a large loss difference due to the via placement. Fig. 18(a) shows the current vector density of prototype 1, and Fig. 18(b) shows that of prototype 3. Prototype 1 has a concentrated current due to the concentrated via placement. On the other hand, prototype 3 suppresses current concentration by dispersing the vias. Although the proximity effect assumed in Fig. 5 occurred, no clear differences were observed due to the via configuration.

Fig. 19(a) shows the current vector density of prototype 3, and Fig. 19(b) shows that of prototype 4. By dispersing the vias away from the rectifier elements, the changes in the current vectors flowing from the vias become more gradual, further suppressing the proximity effect.

Furthermore, it was found that the loss of connection pins passing through vias accounted for only about 2% of the total loss in all prototypes, so it is not necessary to place vias unnecessarily.

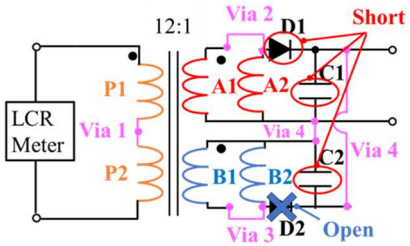


Fig. 14 Experimental circuit diagram

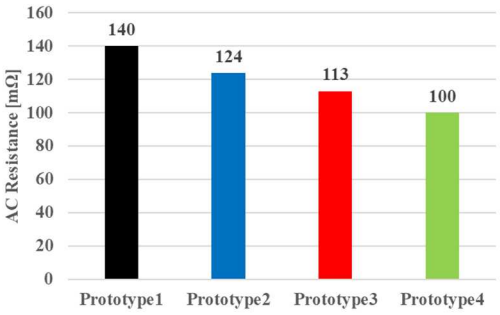


Fig. 15 Comparison of increase in AC resistance

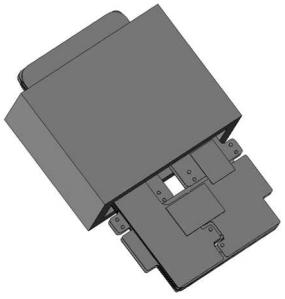


Fig.16 Analysis model

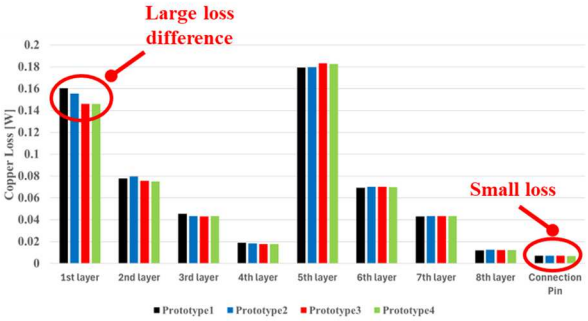
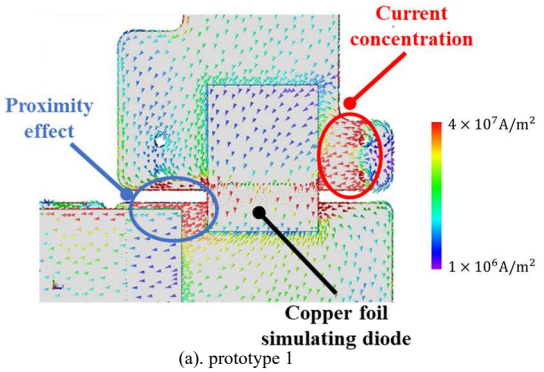
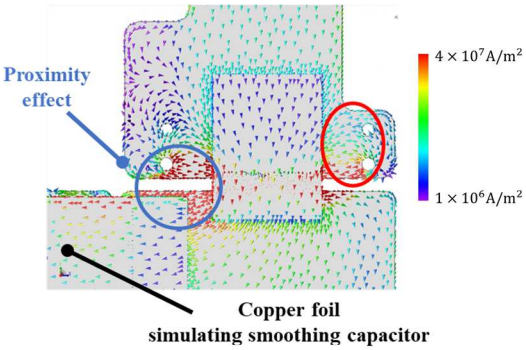


Fig.17 Breakdown of losses for each layer between prototype 1 and 4

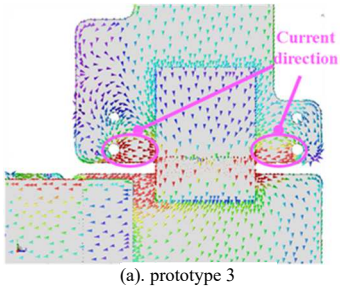


(a). prototype 1

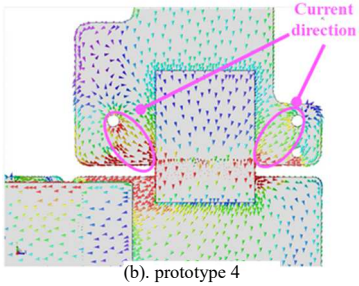


(b). prototype 3

Fig.18 Current vector density of prototype 1 and 4



(a). prototype 3



(b). prototype 4

Fig.19 Current vector density of prototype 3 and 4

V. Experiment and Electromagnetic Field Analysis of PCB Spacing

In this section, prototypes 1 to 4 with d = 0.125 mm and prototypes 5 to 8 with d = 1.0 mm are compared through experiments and simulations.

A. Experiment

In the experiment, the AC resistance of prototypes 5 to 8 was measured to verify the effect of PCB spacing on loss. As shown in Fig.14, LCR meter (nf circuit diagram block ZM2376) was connected to the primary side of the prototypes, and the AC resistance was measured five times at 1 MHz with the secondary side short-circuited, and the average value was calculated.

Fig. 20 shows the comparison results for prototypes 1 to 8. The AC resistance of the prototypes with d = 1.0 mm was smaller than that of the prototypes with d = 0.125 mm. In placement 1 with the largest difference, the AC resistance decreased by approximately 6% from 642 mΩ to 602 mΩ, while in placement 4 with the smallest difference, the AC resistance decreased by approximately 2% from 602 mΩ to 589 mΩ. Despite widening the PCB spacing, the AC resistance decreased. Therefore, it is expected that factors other than the losses generated by the vias themselves have caused this difference.

B. Electromagnetic field analysis

In this section, we analyze the mechanism of loss differences due to PCB spacing using analysis model (d=0.125mm,1.0mm both) in Fig.16. [19] discusses how the current distribution of parallel windings changes depending on the spacing between winding layers. Therefore, we used JMAG to calculate the current distribution of the secondary winding when a 1Arms sinusoidal current was applied to the primary winding.

Fig. 21(a) shows the current distribution in the secondary windings of prototypes 1 to 4, and Fig. 21(b) shows that of prototypes 5 to 8. From Fig. 21, it can be seen that widening the PCB spacing improves the current distribution. Furthermore, Fig. 22 shows the current density in the secondary windings of prototypes 1 and 5. As the current distribution changed, the overall current level of the windings also changed. However, the concentration of current at the edges remained almost the same. In other words, the eddy current assumed in Fig. 4 did not occur significantly. Therefore, the primary cause of the reduced AC resistance by widening the PCB spacing is likely due to the improved current distribution in the secondary windings. From the above, it was found that there is a trade-off relationship between the size of the transformer and its losses.

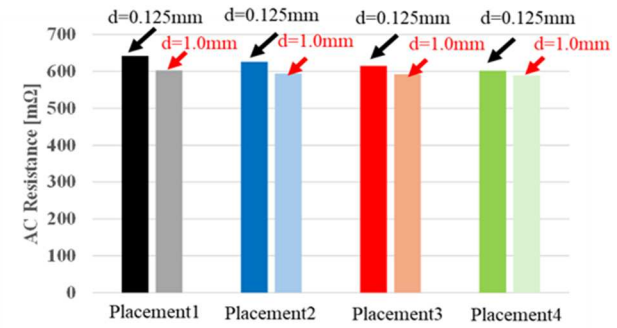
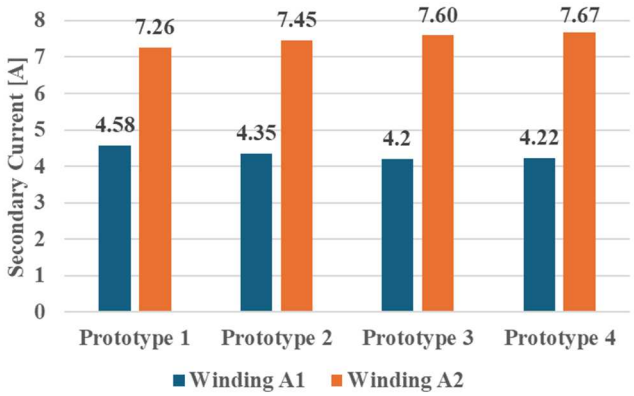
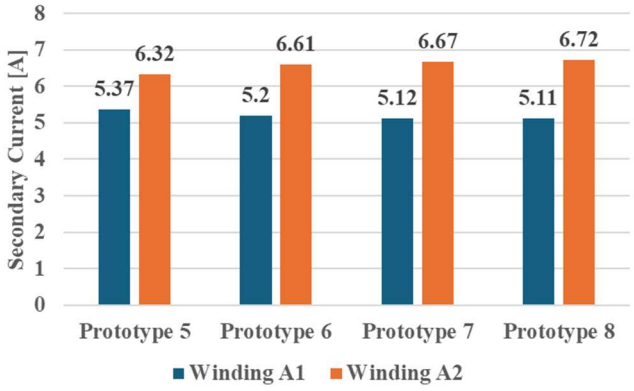


Fig.20 Comparison of AC resistance between prototype 1 and 8

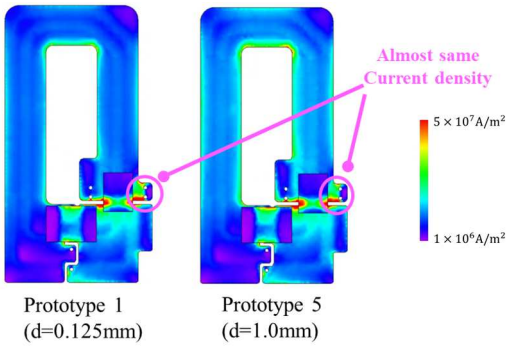


(a). Prototype 1 to 4 (d=0.125mm)

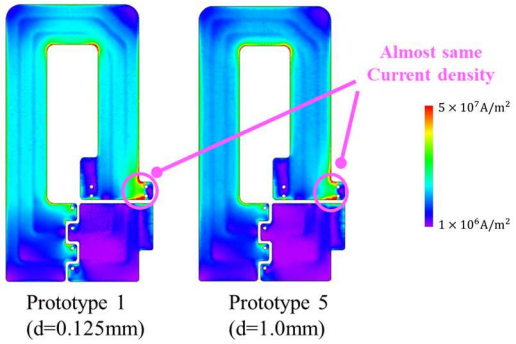


(b). Prototype 5 to 8 (d=1.0mm)

Fig.21 Comparison of current distribution between prototypes with different PCB spacing



(a). Winding A1



(b). Winding A2

Fig.22 Current density of prototype 1 and 5

VI. Conclusion

This study provided several strategies for vertically stacked PCBs transformer. First, dispersing the vias near the rectifier elements can significantly reduce losses. Second, there is a trade-off between PCB spacing and losses. Finally, it is not necessary to place more vias than necessary since the losses of the vias themselves account for only a small portion of the total losses. The analyzed loss difference in this study accounts for only about 2~6 percent of the total loss. However, as power levels increase further, the width of the windings will increase, and these issues are expected to become more remarkable.

Acknowledgment

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