Feasibility of parasitic drain inductance design for minimizing switching loss in bridge circuits using GaN-FETs

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Published in: 2021 IEEE 30th International Symposium on Industrial Electronics (ISIE)

DOI: 10.1109/ISIE45552.2021.9576373

Feasibility of Parasitic Drain Inductance Design for Minimizing Switching Loss in Bridge Circuits Using GaN-FETs

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***Abstract*—Gallium-nitride-field-effect transistors (GaN-FETs) are expected as a key component to the power density improvement of switching power converter for electric vehicles (EVs) because of their low on-resistance and fast switching capability. It is well known that the switching loss is influenced by the drain inductance, which is the parasitic inductance of the power loop, and can be minimized in principle by an appropriate design of the drain inductance. However, in conventional Si-based switching power converters, it is usually difficult to design the drain inductance so that the switching loss minimizes because an appropriate drain inductance becomes too large, thus resulting in large surge voltages of the switching device. On the other hand, this may not be the case when using the GaN-FETs because the inductance that can minimize the switching loss may become small due to the high-*di*/*dt* switching. Therefore, the purpose of this study is to show the feasibility of the parasitic drain inductance design that the switching loss of the GaN-FET in the bridge circuit can be minimized while keeping the surge voltage of the GaN-FET within acceptable limits. The appropriateness of this insight is verified by simulation.**

Keywords—GaN-FET, switching loss, parasitic inductance, stray inductance, power loop

I. INTRODUCTION

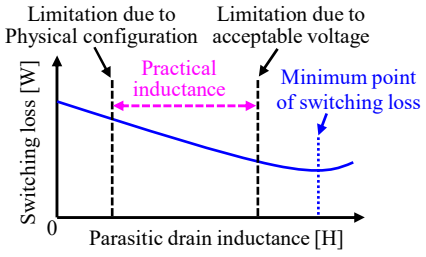
Recently, the gallium-nitride-field-effect transistors (GaN-FETs) have attracted significant attention as a promising next-generation switching device. The GaN FETs can achieve low on-resistance with maintaining high switching speed over the tradeoff limitation of Si-based devices such as the Si-MOSFET and the Si-IGBT [1]. Therefore, the GaN-FETs are expected to contribute to the miniaturization and the efficiency improvement of switching power converters for various applications such as electric vehicles (EVs) [2], [3].

However, due to high-speed switching with high-*di*/*dt*, switching characteristics of the GaN-FET in a switching power converter are significantly influenced by stray (parasitic) inductances existing in printed circuit boards (PCBs), busbars, and circuit components including the GaN-FET. The high-speed switching with high-*di*/*dt* induces large voltage spikes across parasitic inductances. These voltage spikes may cause false triggering [4], [5] or an increase in the switching loss of the GaN-FET [6]–[10]. For solving these problems, the preceding studies [4], [5] proposed the design method of the common-source inductance [11], which is the parasitic inductance of the source terminal, to avoid the false triggering. Furthermore, the preceding studies [6], [10] discussed the relationship between the switching loss and the parasitic inductances to suppress an increase in the switching loss. According to [1] and [9], an increase in the common-source inductance significantly increases the switching loss. Thus, [1] and [9] pointed out that the common-source inductance should be reduced to reduce the switching loss.

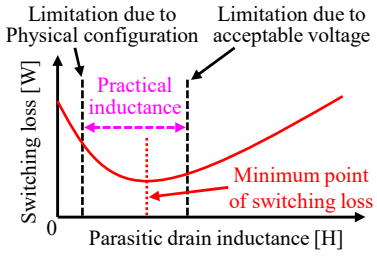
However, as pointed in [8], [10], the switching loss is also relatively influenced by the drain inductance, which is the parasitic inductance of the power loop [6], [12]. Furthermore, the switching loss cannot be necessarily reduced by reducing the drain inductance. Actually, the spike voltage across the drain inductance increases the turn-off loss but decreases the turn-on loss [8]. Besides, as the drain inductance approaches zero, the turn-off loss tends to be larger than the turn-on loss, as shown in [8] and [13]. Therefore, it is obvious that the switching loss is minimized at a certain drain inductance which is not zero. In other words, the switching loss can be minimized by an appropriate design of the drain inductance at a given common-source inductance.

However, in conventional switching power converters using low-speed switching devices such as the Si-MOSFET, it is usually difficult to design the drain inductance to minimize the switching loss. As shown in Fig. 1 (a), in switching power converters using low-speed switching devices, the value of the inductance which can minimize the switching loss tends to become large. A large inductance is not practically acceptable because it causes large surge voltages across the switching devices. In fact, in the preceding study [8], to keep the surge voltage smaller than the rated voltage of the switching devices, the drain inductance is designed to be smaller than the value that minimize the switching loss. Therefore, from the surge voltage point of view, it is usually undesirable to design the drain inductance to minimize the switching loss.

However, this may not be the case when using high-speed switching devices (e.g., GaN-FET). In other words, GaN-based switching power converters have the potential that can



(a) Low-speed switching devices (e.g., Si-MOSFET).



(b) High-speed switching devices (e.g., GaN-FET).

Fig. 1. Hypothesis of relationship between range of practical inductance and minimum point of switching loss.

minimize the switching loss while keeping the surge voltage of the switching device within acceptable limits. This is because the drain inductance that can minimize the switching loss probably may become small as the switching speed (i.e., *di*/*dt*) becomes high, as shown in Fig. 1 (b). As a result, the drain inductance that can minimize the switching loss may exist within the range of the practical inductance. In Fig. 1, the lower limit of the practical inductance in Fig. 1 (b) is lower than that of Fig. 1 (a) because the high-speed switching devices can reduce the size of switching power converters compared to low-speed switching devices. Furthermore, the higher limit of the practical inductance in Fig. 1 (b) is lower than that of Fig. 1 (a) because the surge voltage become large even with a smaller inductance due to high-*di*/*dt* switching.

Therefore, the purpose of this paper is to show that GaN-based switching power converters can minimize the switching loss even when the drain inductance is kept in the range of the practical drain inductance, which is shown in Fig. 1 (b). To achieve this purpose, the remainder of this paper is structured into three sections. Section II reviews the relationship between the switching loss and the drain inductance based on [7]. Furthermore, Section II explains the reason that the inductance that can minimize the switching loss becomes small as the *di*/*dt* becomes high. Section III presents simulation result to verify the appropriateness of Fig. 1 (b). Finally, Section IV gives the conclusions.

II. Relationship among Switching Loss, Drain Inductance, and Switching Speed

For the analysis and simulation, this paper adopts the double-pulse test circuit as a representative example of the bridge circuit. Fig. 2 shows the simplified circuit configuration of the double-pulse test circuit, where S_1 and S_2 are the GaN-FETs, R_{g1} and R_{g2} are the gate resistances, L_{g1} and L_{g2} are the parasitic gate inductances, L_{s1} and L_{s2} are the common source inductances, L_d is the parasitic drain inductance, L_{load} is the inductance of the inductive load, C_i is the capacitance of the input capacitor, V_{in} is the input DC voltage, and r_d is the parasitic resistance of the power loop. In Fig. 2, parasitic inductances of the power loop except the

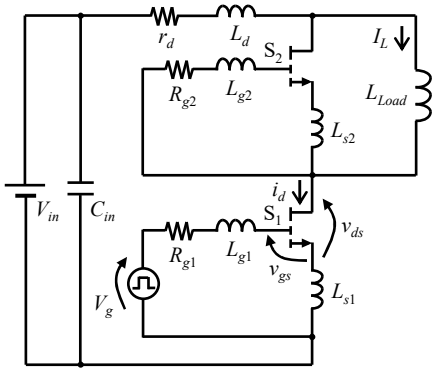
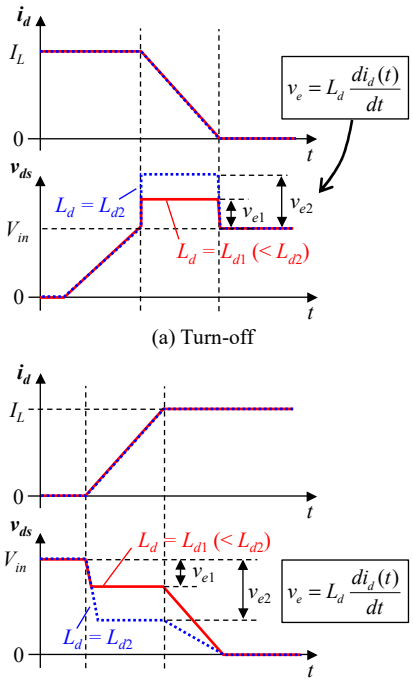


Fig. 2. Simplified circuit configuration of double-pulse test circuit.



(a) Turn-off

(b) Turn-on

Fig. 3. Simplified turn-on and turn-off waveforms of Fig. 2 considering L_d.

common source inductances are aggregated and denoted as L_d for simplicity.

First, based on [7], this section discusses the relationship between the drain inductance L_d and the turn-off loss or the turn-on loss. Fig. 3 shows simplified turn-on and turn-off waveforms of Fig. 2 considering the influence of the drain inductance, where v_{ds} is the drain-to-source voltage of S_1; i_d is the drain current of S_1. In Fig. 3, the red solid lines show the waveforms when $L_d = L_{d1}$ and the blue broken lines show the waveforms when $L_d = L_{d2}$, where $L_{d1} < L_{d2}$. Electromagnetic force (EMF) is generated in the drain inductance during the turn-on and turn-off of the switching device. As shown in Fig. 3 (a), during the turn-off, the EMF increases the voltage across the switching device. Because the switching loss is the time integral of the product of voltage and current, the turn-on loss increases. Therefore, the drain inductance increases the turn-off loss. On the other hand, as shown in Fig. 3 (b), during the turn-on, the EMF decreases the voltage across the switching device. Hence, the drain inductance decreases the turn-on loss.

The dependence of the switching loss (i.e., the sum of the turn-on loss and turn-off loss) on L_d is determined by the magnitude relation between the turn-on loss and the turn-off

loss. However, usually, the larger the reduction of the turn-on loss by increasing L_d is, the smaller the value of L_d at which the switching loss is minimized. As shown in Fig. 3 (b), the EMF increases as the switching speed (i.e., di/dt) increases. Therefore, when fast switching devices are used, the turn-on loss decreases more rapidly with increasing L_d than when slow switching devices are used. Consequently, in the half-bridge circuit with high-speed switching devices, L_d at which the switching loss is minimized becomes small.

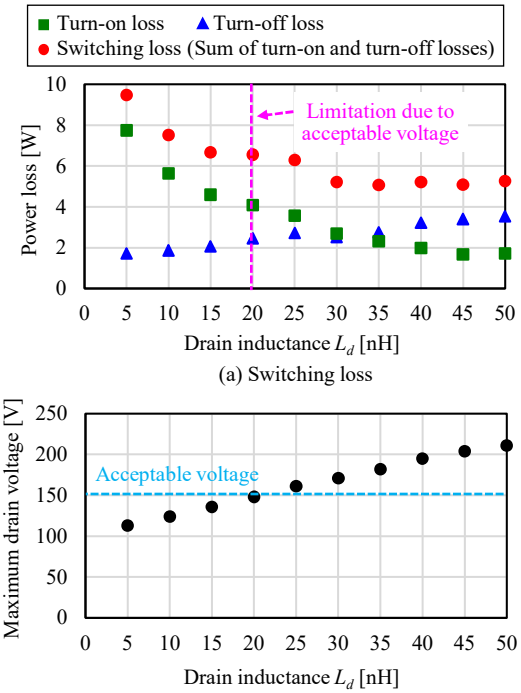
III. Simulation

This section carries out the simulation to verify that the half-bridge circuit with high-speed switching devices can minimize the switching loss even when the drain inductance is kept in the range of the practical drain inductance. In this section, OrCAD PSpice ver. 17.2 was adopted as a circuit simulator.

The simulated circuit is Fig. 2. Furthermore, Table I shows the circuit parameters for the simulation. As shown in Table I, we adopted EPC2207, manufactured by Efficient Power Conversion Corporation, as S_1 and S_2. The Spice model of EPC2207 was provided by the manufacturer. The maximum acceptable voltage for S_1 and S_2 is assumed to be 150 V, which is 75% of the rated voltage of EPC2207 (200 V). In Table I, R_{g1}, R_{g2}, L_{g1}, L_{g2}, L_{s1}, and L_{s2} do not include the internal parasitic resistances or inductances in EPC2207. In the simulation, the switching losses at three different gate resistance (R_g) values (30 Ω, 10 Ω, and 3 Ω) were evaluated. By changing R_g, we adjusted the switching speed. In other words, the simulation results when R_g = 30 Ω emulates the

TABLE I. Circuit Parameters for Simulation

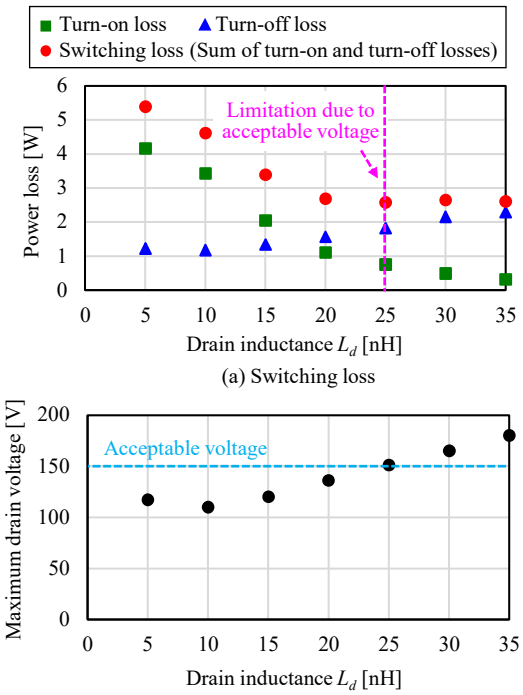
Symbols / Parameters		Values or type number
$S_{1,2}$	Power devices (GaN-FETs)	EPC2207
R_{g1}	Gate resistances for high side	0 Ω
L_{g1}	Parasitic gate inductances for high side	0 nH
L_{s1}	Common source inductances for high side	0 nH
L_{g2}	Parasitic gate inductances for low side	5.0 nH
L_{s2}	Common source inductances for low side	0.5 nH
L_{Load}	Load inductance	20.0 μF
r_d	Parasitic resistance of power loop	100 mΩ
V_{in}	Input DC voltage	100 V
V_g	Gate voltage	−2 to 5 V
I_L	Load current	10 A



(a) Switching loss

(b) Maximum drain voltage

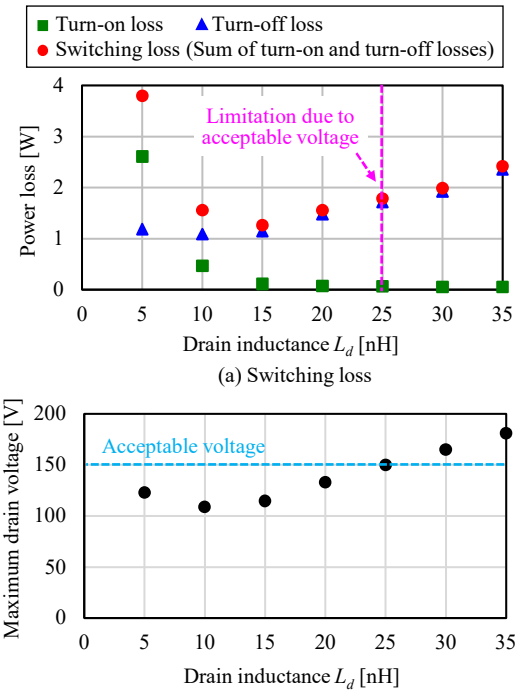
Fig. 4. Simulation results for R_g = 30 Ω.



(a) Switching loss

(b) Maximum drain voltage

Fig. 5. Simulation results for R_g = 10 Ω.



(a) Switching loss

(b) Maximum drain voltage

Fig. 6. Simulation results for R_g = 3 Ω.

results of the half-bridge circuit using low-speed switching devices such as Si-MOSFET. Besides, the simulation results when R_g = 3 Ω emulates the results of the half-bridge circuit using high-speed switching devices such as GaN-FET.

Figs. 4–6 show the simulation results of the maximum drain voltage during turn-off operation and switching loss of S_2 for each R_g. As explained in Section II, the turn-off loss increases with the increase of L_d. Besides, the turn-on loss decreases with the increase of L_d. As shown in Figs. 4–6, the L_d at which the switching loss is minimized when R_g is 30 Ω, 10 Ω, and 3 Ω is 35 nH, 25 nH, and 15 nH, respectively. In other words, as discussed in Section II, the L_d at which the switching loss is minimized decreases as the switching speed increases. This is because the turn-on loss decreases rapidly with the increase of L_d when the switching speed is high. When R_g = 30 Ω, if L_d is set to 35 nH, the maximum drain voltage of S_2 exceeds the limit of the acceptable voltage of EPC2207. On the other hand, when R_g = 3 Ω, if L_d is set to 15 nH, the maximum drain voltage of S_2 does not exceed the limit of the allowable voltage, and the switching loss can be minimized. From the above results, it was verified that the half-bridge circuit using high-speed switching devices can minimize the switching loss while keeping the maximum drain voltage below the acceptable limit. The reason for that the maximum drain voltage when R_g = 3 Ω is smaller than the maximum drain voltage when R_g = 30 Ω will be discussed in the final paper.

IV. Conclusions and Future Works

In conventional Si-based switching power converters, it is practically difficult to design the drain inductance so that the switching loss of the switching devices minimize. This is because the value of the drain inductance minimizing the switching loss tends to be large, resulting in large surge voltages in the switching device. Therefore, in this paper, we investigated whether this common knowledge for Si-based switching power converters also applies to GaN-based switching power converters by using the simulation. As a result, it was found that the parasitic drain inductance design to minimize the switching loss of the GaN-FETs in the bridge circuit while ensuring that the surge voltage does not exceed the acceptable limit is sufficiently feasible. In the final paper, we will add experimental results to support this insight. Furthermore, we will discuss the design method of the drain inductance value.

References

[1] A. Nakajima, K. Takao, and H. Ohashi, "GaN power transistor modeling for high-speed converter circuit design," *IEEE Trans. Electron Devices*, vol. 60, no. 2, pp. 646–652, Feb. 2013.

[2] N. Keshmiri, D. Wang, B. Agrawal, R. Hou, and A. Emadi, "Current status and future trends of GaN HEMTs in electrified transportation," *IEEE Access*, vol. 8, pp. 70553–70571, Apr. 2020.

[3] P. He, A. Mallik, A. Sankar, A. Khaligh, "Design of a 1-MHz high-efficiency high-power-density bidirectional GaN-based CLLC converter for electric vehicles," *IEEE Trans. Veh. Technol.*, vol. 68, no. 1, pp. 213–223, Jan. 2019.

[4] K. Umetani, R. Matsumoto, and E. Hiraki, "Prevention of oscillatory false triggering of GaN-FETs by balancing gate-drain capacitance and common-source inductance," *IEEE Trans. Ind. Appl.*, vol. 55, no. 1, pp. 610–619, Jan.–Feb. 2019.

[5] Y. Hatakenaka, K. Umetani, M. Ishihara, and E. Hiraki, "Optimization of common source inductance and gate-drain capacitance for reducing gate voltage fluctuation after turn-off transition," in *Proc. IEEE Energy Convers. Congr. Expo.* (ECCE 2020), Detroit, MI, USA, 2020, pp. 3155–3162.

[6] P. Nayak and K. Hatua, "Modeling of switching behavior of 1200 V SiC MOSFET in presence of layout parasitic inductance," in *Proc. IEEE Int. Conf. Power Electron. Drives Energy Syst.* (PEDES 2016), Trivandrum, India, 2016, pp. 1–6.

[7] Y. Shen, J. Jiang, Y. Xiong, Y. Deng, X. He, and Z. Zeng, "Parasitic inductance effects on the switching loss measurement of power semiconductor devices," in *Proc. IEEE Int. Symp. Ind. Electron.* (ISIE 2006), Montreal, QC, Canada, 2006, pp. 847–852.

[8] K. wada and M. Ando, "Switching loss analysis of SiC-MOSFET based on stray inductance scaling," in *Proc. Int. Power Electron. Conf.* (IPEC-Niigata 2018-ECCE Asia), Niigata, Niigata, Japan, 2018, pp. 1919–1924.

[9] Z. Chen, D. Boroyevich, and R. Burgos, "Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics," in *Proc. Int. Power Electron. Conf.* (IPEC-Sapporo 2010-ECCE Asia), Sapporo, Hokkaido, Japan, 2010, pp. 164–169.

[10] S. Hain, M.-M. Bakran, C. Jaeger, F.-J. Niedernostheide, D. Domes, and D. Heer, "The effect of different stray inductances on the performance of various types of IGBTs — Is less always better?," in *Proc. Eur. Conf. Power Electron. Appl.* (EPE 2015), Geneva, Switzerland, 2015, pp. 1–9.

[11] K. Umetani, K. Aikawa, and E. Hiraki, "Straightforward measurement method of common source inductance for fast switching semiconductor devices mounted on board," *IEEE Trans. Ind. Electron.*, vol. 64, no. 10, pp. 8258–8267, Oct. 2017.

[12] K. Wang, X. Yang, H. Li, H. Ma, X. Zeng, and W. Chen, "An analytical switching process model of low-voltage eGaN HEMTs for loss calculation," *IEEE Trans. Power Electron.*, vol. 31, no. 1, pp. 635–647, Jan. 2016.

[13] A. Nakajima, K. Takao, and H. Ohashi, "Power loss characterization and modeling for GaN-based hard-switching half-bridges considering dynamic on-state resistance," *IEEE Trans. Transport. Electrific.*, vol. 6, no. 2, pp. 540–553, June 2020.