Evaluation of impact of parasitic magnetic coupling in PCB layout on common source inductance of surface mounted package

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Abstract- **Recently, the common source inductance (CSI) is regarded as one of the most important obstacles for achieving ultrafast switching of switching converters. The CSI is pointed out to be a major cause of deterioration of the switching speed and false triggering. Therefore, many design instructions of next generation switching devices, such as GaN-FETs and SiC-MOSFETs, have pointed out the necessity to reduce the CSI. Certainly, many of the next generation switching devices are provided in surface mount packages in order to enable PCB designers to minimize the CSI by eliminating the common source path. However, the parasitic magnetic coupling between the gating circuit and the power circuit may still add the CSI, although preceding studies have scarcely reported how greatly the PCB layout can affect the CSI and the switching waveforms. This paper experimentally evaluated the impact of the parasitic magnetic coupling of the PCB layout on the CSI of the surface mount package and on the switching waveforms. As a result, the parasitic magnetic coupling was found to cause the major difference in the CSI. In addition, large difference in the turn-off switching waveforms was found to be caused by the difference in the magnetic coupling. The reason is also analyzed and discussed in this paper, suggesting importance of appropriate design of the parasitic magnetic coupling in the PCB layout.**

I. INTRODUCTION

The recent progress of the semiconductor technology has given rises to fast switching semiconductor devices, such as SiC-MOSFETs and GaN-FETs. These devices are emerging as promising switching devices for power converters. Owing to their fast switching capability, the size of passive components can be reduced by high frequency operation and the efficiency can be improved by reduction of the switching loss.

However, fast switching often generates large noise voltage due to the common source inductance (CSI). The CSI is the parasitic inductance of the common source path, which is the wiring path shared by the gating circuit and the power circuit [1]–[4]. At the turn-on, a sudden change in the current occurs at the source terminal. As a result, an instantaneous noise voltage is inducted at the CSI. This noise voltage overlaps with the gate-source voltage. Hence this noise voltage may lower the gate-source voltage at the switching transition, thus deteriorating the switching speed and increasing the switching loss [1]. In addition, this noise voltage may cause the false triggering or the false turn-on, such as the self-turn-on [3]–[7]. Therefore, many application notes have pointed out that minimizing the CSI is essential for achieving fast switching [8][9].

In order to minimize the CSI, many of next generation switching devices become commonly provided in surface mount packages. Compared with through-hole packages, surface mount packages tend to have extremely small wiring length for the source terminal. The source terminal inevitably adds the common source path that cannot be eliminated by the PCB design. As a result, the surface mount packages enables drastic elimination of the common source path; and therefore, these packages are effective for reducing the CSI.

Nonetheless, elimination of the common source path does not necessarily indicate complete elimination of the CSI. As discussed in the next section, the parasitic magnetic coupling between the gating circuit and the power circuit can work as an additional common source inductance [10][11]. Because the magnetic coupling can take either the positive or negative polarity, the total CSI can be increased or decreased according to the polarity of the magnetic coupling.

A previous study [10] have revealed that the CSI can be reduced by adding a discrete transformer to implement negative magnetic coupling between the gating circuit and the power circuit. However, adding a discrete transformer also adds significant leakage inductance to both of the gating circuit and the power circuit, which may be hazardous for causing severe self-turn-on or severe switching surge under fast switching.

On the other hand, the parasitic magnetic coupling of the wiring paths in the PCB layout can also be used to add or reduce the CSI. Nonetheless, this parasitic magnetic coupling is generally weak compared with a discrete transformer. As for the through-hole package, the effect of the parasitic magnetic coupling has been regarded to be generally far smaller compared with the CSI contributed by the inductance of the source terminal. However, if the common source path is entirely eliminated by appropriate design of the PCB layout and utilization of a surface mount package, as is often the cases in the next generation switching devices, the parasitic magnetic coupling may have significant influence on the CSI and therefore on the switching. This idea may be important for the power converter design using next generation switching devices because the parasitic magnetic coupling may become a major design consideration of the PCB design.

The purpose of this paper is to evaluate the impact of the parasitic magnetic coupling of the PCB layout on the CSI of surface mount packages as well as on the switching waveforms. This paper evaluated the CSI of a surface mount package
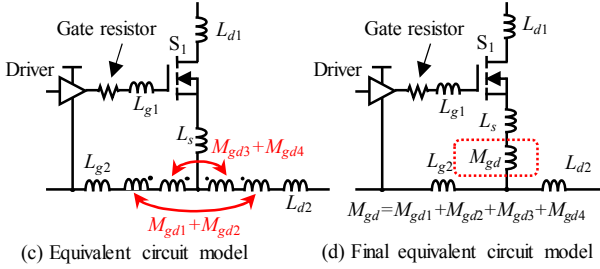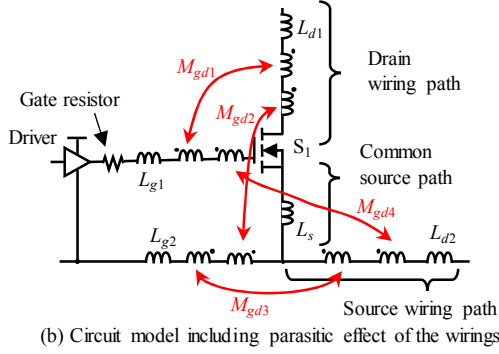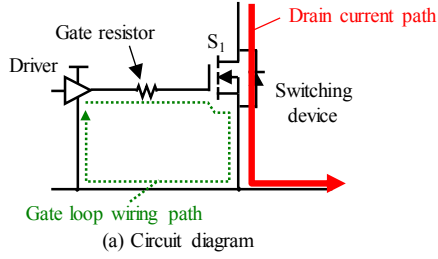
(a) Circuit diagram

(b) Circuit model including parasitic effect of the wirings

(c) Equivalent circuit model

(d) Final equivalent circuit model

$$M_{gd}=M_{gd1}+M_{gd2}+M_{gd3}+M_{gd4}$$

Fig. 1. Derivation of the equivalent circuit model of a switching device with a gate driver. Transformers M_{gd1}–M_{gd4} are ideal transformers without leakage inductance.

Transformer
(The turn ratio is 1:1.)
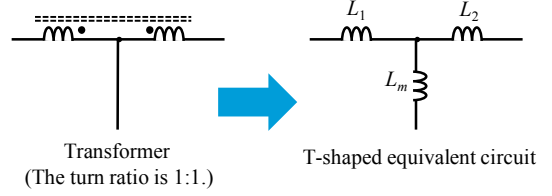
T-shaped equivalent circuit

Fig. 2. T-shaped equivalent circuit model of a transformer with leakage inductance.

II. ANALYSIS OF EFFECT OF PARASITIC MAGNETIC COUPLING ON COMMON SOURCE INDUCTANCE

The magnetic coupling between the gating circuit and the power circuit is equivalent to the CSI. This section reviews the reason using a simple circuit model of a switching device with a gate driver shown in Fig. 1(a). In order to discuss the effect of the parasitic inductance and the parasitic magnetic coupling of the wiring paths, we add inductors and transformers to the circuit model, obtaining Fig. 1(b). Inductors L_{d1}, L_{d2}, L_{g1}, and L_{g2} represent the parasitic inductance of the wiring. Inductor L_s is the parasitic inductance of the common source path, which contributes to the CSI. Transformers M_{gd1}–M_{gd4} represent the mutual inductance of the magnetic coupling between the gating circuit and the power circuit. Specifically, M_{gd1} and M_{gd2} are the mutual inductance between the drain wiring and the gate loop wiring path and M_{gd3} and M_{gd4} are that between the gate loop wiring path and the source wiring, respectively. These transformers are ideal. Hence, M_{gd1}–M_{gd4} do not have the leakage inductance.

Note that the current of the drain wiring path is equal to that of the source wiring. Hence, the drain-side winding of the transformers M_{gd1} and M_{gd2} can be equivalently moved onto the source wiring path, if we only discuss the effect of the power circuit on the gating circuit, i.e. the voltage induction in the gating circuit generated by the power circuit. Furthermore, the gate driver connects the gate to the source terminal directly during the off-state of S_1 and via the decoupling capacitor of the gate driver during the on-state of S_1. Hence, the gate-side winding of M_{gd1} and M_{gd4} can also be equivalently moved onto the wiring path from the GND terminal of the gate driver to the source terminal of S_1, if we only discuss the AC voltage induction in the gating circuit. Consequently, we obtain the equivalent circuit as shown in Fig. 1(c).

As widely known, a transformer with the same number of turns for the primary and secondary windings can be expressed as a T-shaped equivalent circuit of three independent inductors, as shown in Fig. 2. Inductor L_1 and L_2 represent the leakage inductance of the primary and secondary windings, respectively, whereas L_m represents the mutual inductance. As for Fig. 1(c), $M_{gd1}+M_{gd2}$ and $M_{gd3}+M_{gd4}$ are assumed to be ideal transformers without leakage inductance. Therefore, these transformers are equivalent to independent inductors attached on the common source path. Hence, Fig. 1(b) can be equivalently expressed as Fig. 1(d).

As can be seen in Fig. 1(d), the mutual inductance M_{gd1}–M_{gd4} work as the CSI, similarly as L_s. Certainly, these mutual

mounted on the PCB and investigated how greatly the PCB layout can affect the CSI according to the parasitic magnetic coupling between the gating circuit and the power circuit. Furthermore, the switching waveforms are also compared under various polarity and intensity of the magnetic coupling in order to evaluate how greatly the PCB layout can affect the switching waveforms.

Certainly, next generation switching devices are provided in various surface mount packages. However, it is difficult to pick up a typical package from these packages because next generation switching devices have little history of mass production. Therefore, this paper evaluates the CSI using a typical surface mount package of a Si-based power MOSFET.

The following discussion consists of 4 sections. Section II presents a brief explanation why the parasitic magnetic coupling increases or decreases the CSI. Then, section III experimentally evaluates the CSI under various polarity and intensity of the parasitic magnetic coupling of the PCBs. Section IV experimentally evaluates the switching waveforms and discusses how greatly the CSI can affect the switching waveforms. Finally, section V gives conclusions.
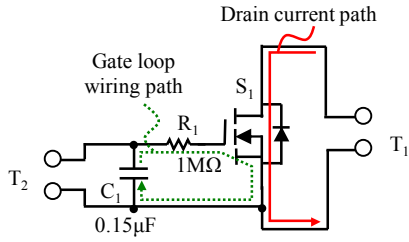
Fig. 3. Circuit diagram of the experimental PCBs for evaluation of the impact of the parasitic magnetic coupling on the common source inductance.

inductance are not related to the common source path. However, we cannot distinguish the effect of these mutual inductance from L_s by means of observation of the circuit behavior. Therefore, this paper regards M_{gd1}–M_{gd4} as fundamental contributors of the CSI, similarly as L_s.

It should be noted that the mutual inductance M_{gd1}–M_{gd4} can have positive or negative value. Therefore, this mutual inductance can increase or decrease the CSI. Furthermore, in a special case in which L_s is extremely small as a result of eliminating the common source path, the CSI can be entirely reduced to be zero or even take a negative value.

III. Evaluation of Impact of Parasitic Magnetic Coupling on Common Source Inductance

A. Evaluation method

This section experimentally evaluates the impact of the parasitic magnetic coupling on the CSI of a typical surface mount package mounted on a PCB. For this purpose, we made five PCBs with various polarity and intensity of the parasitic magnetic coupling. Then, we evaluated and compared the CSI among these experimental PCBs.

Fig. 3 shows the circuit diagram of the experimental PCBs. Each PCB has a MOSFET (S_1), a capacitor (C_1), and a resistor (R_1). Capacitor C_1 and resistor R_1 was used for the CSI measurement. In this measurement, the wiring path from the gate to the source of S_1 via C_1 and R_1 is required to have the same PCB layout as the gating circuit. Hence, this wiring path corresponds to the gate loop wiring path defined in Fig. 1. In addition, the wiring path from one terminal to the other terminal of T_1 via S_1 is required to have the same PCB layout as the power circuit. Hence, this wiring path corresponds to the drain current.

MOSFET S_1 is a Si-based n-channel MOSFET (Fairchild, FDMC86240) with a surface mount package. This MOSFET was employed in this experiment because its package has extremely short terminals. Furthermore, this MOSFET package has three internally connected source terminals. Therefore, we eliminated the common source path (at least, outside the package) by utilizing one source terminal as the Kelvin source terminal. In other words, one source terminal was used to connect to the gating circuit; and the other two source terminals were used to connect to the power circuit. As a result, the gate loop wiring path was separated from the drain current path except for one point.
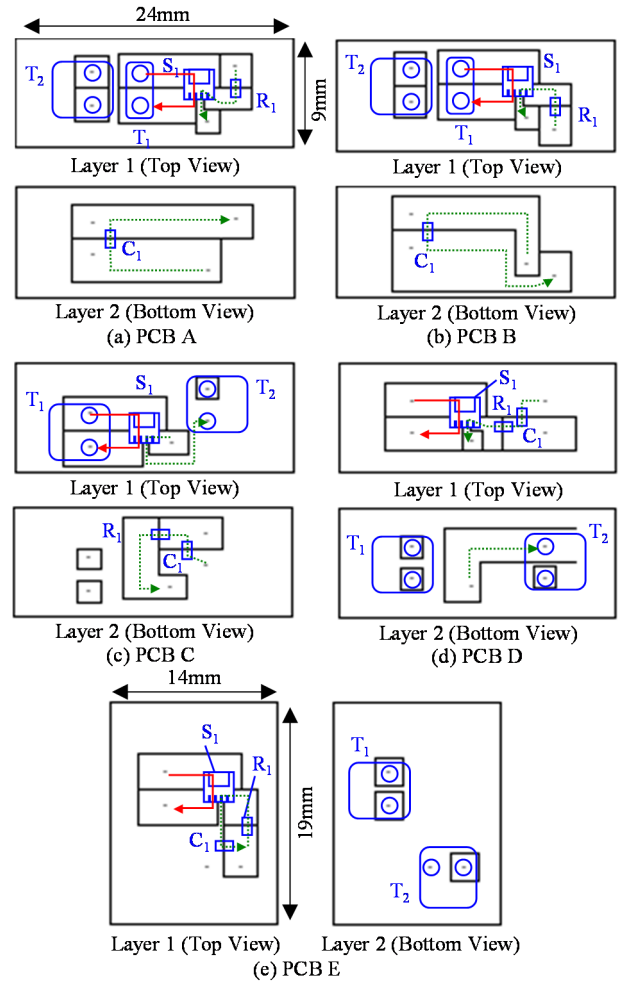

Fig. 4. Experimental PCB layout for evaluation of the impact of the parasitic magnetic coupling on the common source inductance.
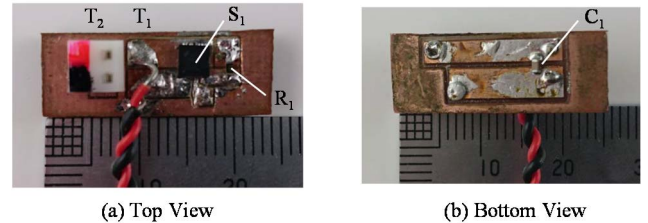

Fig. 5. Photographs of experimental PCB A.

Fig. 4 shows the PCB layout of the experimental PCBs; and Fig. 5 shows the photograph of PCB A. Among these experimental PCBs, the layout was almost the same for the drain current path, although the layout had a variety for the gate loop wiring path. As a result, the parasitic magnetic coupling between the gating circuit and the power circuit had a variety in the polarity and the intensity.

These PCBs had two layers so that the gate loop wiring path had some overlap with that of the drain current path. This overlap is the major contributor of the parasitic magnetic coupling. In the overlapped wirings, the current in one wiring is known to induce the voltage in the other wiring so that the opposite current flows in this wiring. Therefore, the overlapped

TABLE I
POLARITY AND INTENSITY OF THE PARASITIC MAGNETIC COUPLING IN
EXPERIMENTAL PCBs

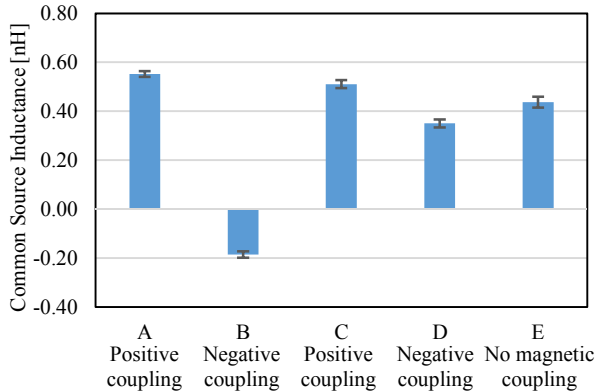| PCB	A	B	C	D	E
Polarity	Positive	Negative	Positive	Negative	-
Intensity	Large	Large	Small	Small	-

Fig. 6. Measurement result of the CSI in the experiment in section III.
For each PCB, The CSI was measured by 4 times at 9 frequencies in 2–
10MHz. This figure plots the mean values. The error bar indicates the
95% confidence interval of the mean.

wiring paths work as a weakly coupled transformer. The
mutual inductance between the wirings are proportional to the
overlapped length. Hence, the polarity and the intensity of the
magnetic coupling was changed by varying the relation of the
current direction and the length of the overlapping wirings.

Table I summarizes the designed difference in the polarity
and the intensity of the parasitic magnetic coupling among the
five experimental PCBs. PCBs A and C were designed to have
the positive magnetic coupling, whereas PCBs B and D were
designed to have the negative magnetic coupling. On the other
hand, PCBs A and B had larger overlapped wiring length
compared with PCBs C and D. PCB E had no overlap between
the gate loop wiring path and the drain current path.

Then, we measured and compared the CSI among these
experimental PCBs. The CSI measurement of the surface
mount packages has long been thought to be difficult because
of its small inductance and its dependence on the parasitic
magnetic coupling. However, [11][12] have recently proposed
a simple but effective CSI measurement method applicable to
an already mounted switching device. We employed this
method for the CSI measurement. Detailed description on the
method is presented in the appendix.

B. Results and Discussion

Fig. 6 shows the result. The CSI values of these PCBs were
small below 1nH. However, a large variety was found in the
CSI. PCBs A and C showed comparatively large CSI compared
with PCBs B and D. Because the layout of PCB E was
designed to be free from the parasitic magnetic coupling, the
CSI of PCB E can be regarded as the intrinsic CSI of this
package. Hence, comparing PCBs A–D with PCB E, we can
find that the positive and negative magnetic coupling
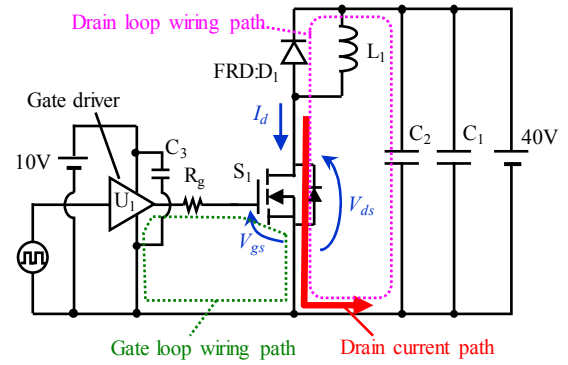corresponded to increase and decrease in the CSI, respectively.

Fig. 7. Circuit diagram of the experimental double pulse tester.

TABLE II
CIRCUIT ELEMENTS IN EXPERIMENTAL DOUBLE PULSE TESTER

S_1	Si-MOSFET FDMC86240 (Fairchild Semiconductor Corp.)
D_1	Fast Recovery Diode RF1501TF3S (ROHM Corp.)
R_g	Chip Resistor 0Ω MCR03EZPJ000 (ROHM Corp.)
C_1	Electrolytic Capacitor 100μF EEUEE2G101 (Panasonic)
C_2	Ceramic Capacitor 1μF×2pcs GRM55DR72E105KWO1L (Murata)
C_3	Ceramic Capacitor 0.15μF GMR188B11E154K (Murata)
L_1	Inductor 100μH
U_1	Gate Driver NCP81074BDR2G (ON Semiconductor)

Furthermore, comparing the deviation from PCB E between
the PCBs with the parasitic magnetic coupling of the same
polarity, we can also find that intense magnetic coupling tends
to have larger deviation than weak magnetic coupling. These
features are consistent with the theory reviewed in section II.
Therefore, the variation in the CSI among the experimental
PCBs can be consistently explained as the result of the parasitic
magnetic coupling of the PCB layout.

The CSI variation among the PCBs had the similar order as
the intrinsic CSI. This fact indicates that the parasitic magnetic
coupling can have a major impact on the CSI of surface mount
packages, if the common source path is entirely eliminated by
the PCB design. Particularly, PCB B showed negative
magnetic coupling. Therefore, the CSI of surface mount
packages can probably be reduced to be zero by appropriate
PCB design considering the parasitic magnetic coupling.

IV.   EVALUATION OF IMPACT OF PARASITIC MAGNETIC
COUPLING ON SWITCHING

A. Evaluation Method

Next, we observed the switching waveforms to evaluate how
greatly the switching is affected by the variation in the CSI
caused by the parasitic magnetic coupling of the PCB layout.
For this purpose, we measured the switching waveforms of the
double-pulse test circuit with four types of the PCB layout.
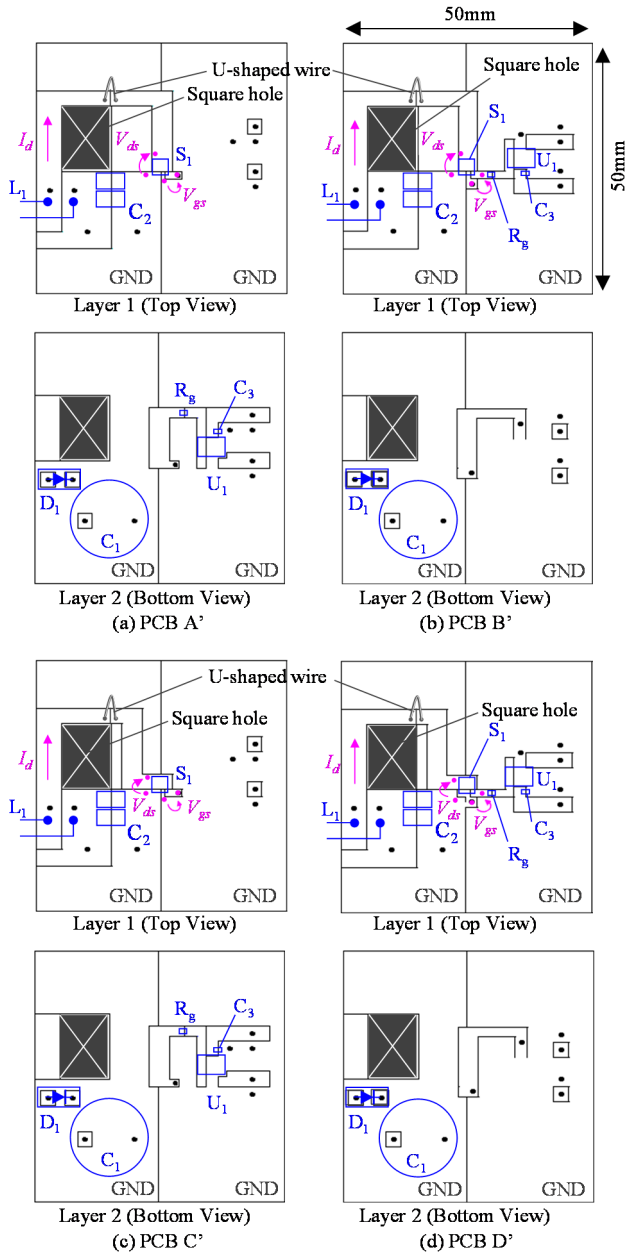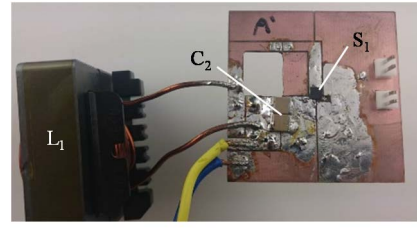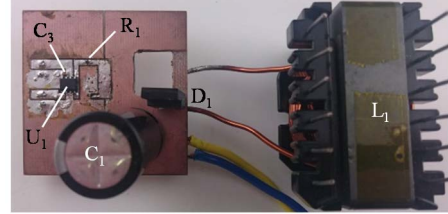
Fig. 8. Experimental PCB layout for evaluation of the impact of the parasitic magnetic coupling on the switching. Square hole was implemented to insert a current probe for measurement of the drain current i_d.

(a) Top View

(b) Bottom View

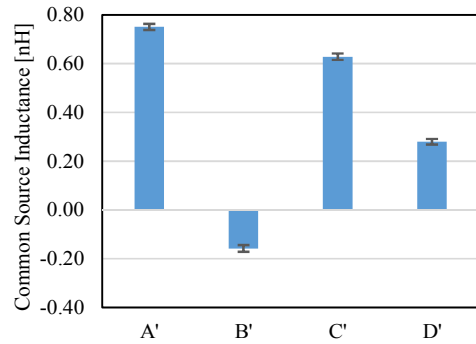Fig. 9. Photograph of experimental PCB A′.

Fig. 10. Measurement result of the CSI in the experiment in section IV. For each PCB, the CSI was measured by 4 times at 9 frequencies in 2–10MHz. This figure plots the mean values. The error bar indicates the 95% confidence interval of the mean.
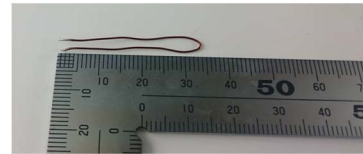

Fig. 11. Photograph of the U-shaped wire used in the experimental PCB.

Fig. 7 shows the circuit diagram of the double-pulse test circuit. The specifications are shown in Table II. In this experiment, we employed the same switching device as that employed in the experiment of section III. Because the voltage tolerance of the switching device was limited, we supplied the circuit with the DC voltage of 40Vdc.

Fig. 8 shows the PCB layout of the experimental PCBs of the double-pulse test circuit; and Fig. 9 shows the photograph of PCB A′. The gate loop wiring was designed to have similar PCB layout near the switching device as those in the experiment of section III. Hence, PCBs A′, B′, C′, and D′ correspond to PCBs A, B, C, and D, respectively, in section III.

We designed the gate loop wiring path and the drain loop wiring path to have similar total length among PCBs A′–D′. As a result, the parasitic inductance of the gate loop wiring path and the drain loop wiring path were almost the same among the experimental PCBs; and the difference was mainly made in the parasitic magnetic coupling.

Table III shows the parasitic inductance of the experimental PCBs; and Fig. 10 shows comparison result of the CSI among
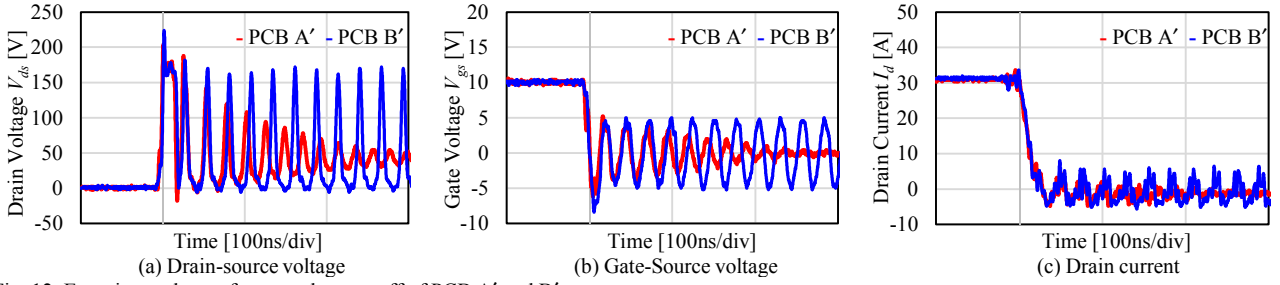
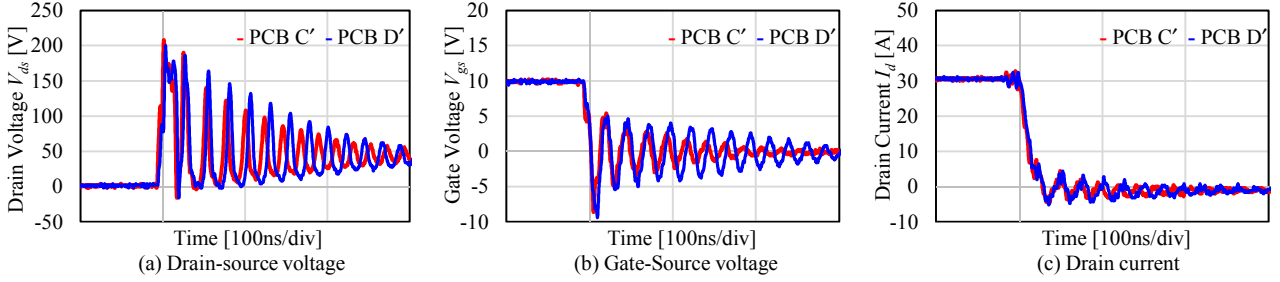Fig. 12. Experimental waveforms at the turn-off of PCB A′ and B′.

Fig. 13. Experimental waveforms at the turn-off of PCB C′ and D′.

the experimental PCBs. The inductance L_g and L_d are the parasitic inductance of the gate loop wiring path and drain loop wiring path, respectively, defined in Fig. 7; and L_{CS} is the CSI. The values of L_g and L_d were obtained by the measurement method described in [13]. The value of L_{CS} was measured using the method reviewed in the appendix, similarly as in section III.

For easy comparison of the switching waveforms, the experimental PCBs were designed to have large switching noise. Therefore, we designed the drain current path to have large parasitic inductance to generate large switching surge in the drain-source voltage of S_1. For this purpose, we inserted a U-shaped wire in the experimental PCBs. The photograph of the U-shaped wire is shown in Fig. 11.

B. Results

In this experiment, we observed the turn-off waveforms when the drain current reached 30A. Fig. 12 and Fig. 13 show the results. In spite of the small CSI below 1nH, a large difference was found among the experimental PCBs in the gate-source voltage and the drain-source voltage, whereas little difference was found in the drain current transition speed. Particularly, in PCB B′, the drain-source voltage as well as the gate-source voltage was continuously oscillated, suggesting self-sustaining repetitive false triggering after the turn-off. On the other hand, in the other PCBs, the drain-source voltage and the gate-source voltage gradually settled down after the turn-off. However, the settling time for PCB D′ was found to be slightly larger than PCB A′ and C′.

It should be noted that these voltage waveforms were more unstable as the CSI becomes smaller. This result is contrary to the common idea that less CSI results in stable switching. The reason of this result is analyzed in the next subsection.

However, this result revealed that the parasitic magnetic coupling can have large impact on the switching.

C. Discussion

The self-sustaining repetitive false triggering found in PCB B′ can also be observed in GaN switching devices [13]. This phenomenon of GaN devices has been analyzed and elucidated to be caused by large noise voltage induction at the gate. This noise voltage induction is caused by the parasitic oscillator formed of S_1, the parasitic inductance, and the parasitic capacitance, which is excited by the turn-off of S_1. Therefore, it is natural to suppose that the unstable switching waveforms found in PCB B′ were also caused by large noise voltage induction in the gate-source voltage. Hence, this subsection analyzes the CSI dependence on the noise voltage in the gate-source voltage.

As widely known, the noise voltage induction at the gate was mainly caused by two parasitic elements: One is the CSI, and the other is the gate-drain capacitance [6]. Now, we analyze the dependence of the CSI on the noise voltage at the gate using a simple model.

We model the high frequency voltage fluctuations after the turn-off of the double-pulse test circuit shown in Fig. 6 using an AC equivalent circuit model. After the turn-off, the DC current of L_1 flows through D_1; and therefore, D_1 can be regarded as short-circuit for the fluctuations. Furthermore, because of the high frequency, L_1 can be regarded as the open-circuit, whereas C_1 and C_2 can be regarded as the short-circuit. The gate driver connects the gate to the source of S_1 after the turn-off. Hence, the gate driver can also be regarded as the short-circuit that connect the gate to the source of S_1. For convenience, we simply model S_1 as a voltage-controlled current source, as in [13].

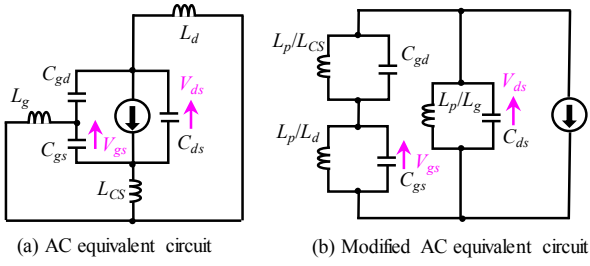(a) AC equivalent circuit   (b) Modified AC equivalent circuit

Fig. 14. Simplified AC equivalent circuit model.

On the other hand, we model the parasitic inductance of the wiring as well as the parasitic capacitance of S_1 as the inductors and capacitors. We attach L_d, L_g, and L_{CS} in series with the drain, the gate, the source of S_1, respectively. Inductance L_d and L_g are the parasitic inductance of the drain loop wiring path and the gate loop wiring path, respectively; L_{CS} is the CSI. Furthermore, we introduce C_{gd}, C_{gs}, C_{ds}, which are the parasitic capacitance between the gate and the drain, between the gate and the source, and between the drain and the source, respectively. As a result, an AC equivalent circuit model for the fluctuations is obtained as shown in Fig. 14(a). (For convenience, we neglected the parasitic resistance of the wiring, the gate driver, the MOSFET, and the diode.)

Applying the Y-Δ transformation to the network of L_d, L_g, and L_{CS}, we can transform Fig. 14(a) into Fig. 14(b), where L_p is defined as

$$L_p = L_{CS} L_d + L_g L_{CS} + L_g L_d . \qquad (1)$$

As a result, the equivalent circuit model consists of three parallel LC resonators and the current source.

We approximate that almost all the current from the current source flows into the LC resonator of C_{ds} and L_p/L_g because the LC resonator of C_{gd} and L_p/L_{CS} tends to have high impedance. Therefore, sudden change in the drain current, i.e. the current from the current source, excites resonance in the LC resonator of C_{ds} and L_p/L_g, causing voltage fluctuation at the resonance frequency of this resonator.

Note that the gate-source voltage and the drain-source voltage corresponds to the voltage across C_{gs} and C_{ds}, respectively. Therefore, this voltage fluctuation in the LC resonator of C_{ds} and L_p/L_g corresponds to the switching noise in the drain-source voltage. The switching noise in the drain-source voltage was attenuated by the voltage divider composed of two parallel LC resonator: One consists of C_{gd} and L_p/L_{CS}; and the other consists of C_{gs} and L_p/L_d. Finally, the output of the voltage divider corresponds to the noise voltage at the gate.

In order to minimize the noise voltage at the gate, the voltage divider is required to have high attenuation at the resonance frequency of C_{ds} and L_p/L_g. Hence, the best design is to set resonance frequency of the high-side LC resonator of the voltage divider at the same frequency as the resonance frequency of C_{ds} and L_p/L_g. Hence, the CSI should satisfy
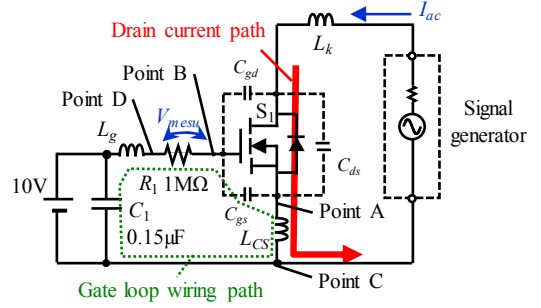

Fig. 15. Circuit diagram of the CSI measurement system.

$$\frac{L_{CS}}{C_{gd}} = \frac{L_g}{C_{ds}} . \qquad (2)$$

Equation (2) indicates that there is an appropriate balance between the two major causes of the noise voltage at the gate, i.e. L_{CS} and C_{gd}. Larger deviation from the balance may result in larger noise voltage at the gate because the attenuation of the voltage divider become worse, and finally large deviation may cause higher susceptibility in repetitive false triggering.

As for the experiment of this section, the appropriate value of L_{CS} for PCBs A′–D′ was calculated as 0.68nH, 0.71nH, 0.65nH and 0.68nH, respectively, according to (2). Therefore, PCBs A′ and C′ were much closer and PCB D′ was slightly closer to the appropriate balance than PCB B′, as can be seen in Table III. Therefore, this appropriate value of CSI can consistently explain the stability in the switching waveforms of PCB A′ and C′ as well as instability of PCB B′.

It should be noted that negative CSI value is not appropriate according to (2). Therefore, the magnetic coupling should probably be designed not to have the negative CSI.

V.   CONCLUSION

Next generation switching devices are commonly provided in surface mount packages. These packages are effective for enabling the PCB designers to eliminate the common source path, thus minimizing the CSI. However, the parasitic magnetic coupling of the PCB layout can also cause additional CSI.

Conventionally, the CSI caused by the parasitic magnetic coupling has been regarded as negligible compared with that by the common source path. However, as for surface mount packages, the parasitic magnetic coupling may have significant effect on the CSI and therefore on the switching.

This paper experimentally evaluated the impact of the parasitic magnetic coupling on the CSI, as well as the switching, of a surface mount package. As a result, the parasitic magnetic coupling was found to be a major contributor of the CSI and can have essential effect on the false triggering at the fast switching. Theoretical analysis suggested that the appropriate balance between the CSI and the gate-drain capacitance of the switching device may be important for

stabilizing the switching waveforms, implying importance of the appropriate design of the parasitic magnetic coupling.

APPENDIX

This appendix briefly reviews the CSI measurement method proposed in [11][12]. Fig. 15 illustrates the circuit diagram of the CSI measurement system, where L_{CS} are the CSI; L_g is the parasitic inductance of the gate loop wiring path defined in Fig. 3 and Fig. 7; L_k is the parasitic inductance of the loop wiring path formed of the signal generator and the switching device; C_1 is a surface mount ceramic capacitor with sufficiently large capacitance than C_{gs}; R_1 is a resistor with far larger resistance than the impedance of C_{gs}, C_1, L_g, and L_{CS}; C_{gd}, C_{gs}, C_{ds} are the parasitic capacitance of the switching device.

The gate loop wiring path and the drain current path should have the same layout as the PCB to be tested. If the gate driver and the gate resistor are mounted on the PCB to be tested, as in the case of the experimental PCBs in section IV, the following process is required to construct the CSI measurement system: 1. the gate driver should be removed; 2. C_1 should be mounted on the PCB pads for the gate driver to connect the output and GND terminals of the gate driver; and 3. the gate resistor is replaced by R_1.

We connect the DC voltage source in parallel to C_1 and supplied sufficient DC voltage to keep S_1 in the on-state. Furthermore, we connect the signal generator to the drain and source terminals of S_1 to provide the AC current.

The voltage induced at L_{CS} cannot be directly measured because point A in Fig. 15 is generally hidden inside the package. However, point B has the same AC voltage level as point A because R_1 has far larger impedance than C_1, L_g, C_{gs}, and L_{CS}. Furthermore, point D has the same AC voltage level as point C according to the same reason. Hence, the voltage drop at R_1 is the same as that at L_{CS}.

By measuring the voltage drop at R_1 and the current supplied from the signal generator, we can calculate the CSI as

$$L_{CS} = \frac{V_{mesu}}{2\pi f I_{ac}} \sin\phi, \qquad (3)$$

where V_{mesu} and I_{ac} are the effective value of the voltage drop at R_1 and the AC current from the signal generator, respectively; f is the frequency of the AC current; and ϕ is the phase difference between the voltage drop at R_1 and the AC current of the signal generator.

In the CSI measurement of this paper, the signal generator was set to supply the AC current of 0.2–0.3Apeak approximately. We measured the CSI of each PCB at nine frequencies from 2MHz to 10MHz. Furthermore, for each frequency, we measured 4 times. As a result, each PCB was measured for 36 times. The CSI value of each PCB was determined by averaging these 36 values. The error bars in Fig.

6 and Fig. 10 represents the 95% confidence interval estimated based on these 36 values.

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