Prevention of oscillatory false triggering of GaN-FETs by balancing gate-drain capacitance and common-source inductance

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Prevention of Oscillatory False Triggering of GaN-FETs by Balancing Gate-Drain Capacitance and Common Source Inductance

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***Abstract* -- GaN-FETs are promising switching devices with fast switching capability. However, they commonly have low gate threshold voltage, suffering from susceptibility to the false triggering. Particularly, the oscillatory false triggering, i.e. a self-sustaining repetitive false triggering, can occur after a fast switching, which is a severe obstacle for industrial applications. The purpose of this paper is to elucidate the design instruction for preventing this phenomenon. The oscillatory false triggering is known to be caused by the parasitic oscillator circuit formed of a GaN-FET, its parasitic capacitance and the parasitic inductance of the wiring. This paper analyzed the non-oscillatory condition of this oscillator. The result revealed an appropriate ratio between the gate-drain capacitance and the common source inductance is a key to prevent the oscillatory false triggering. Experiment successfully verified this analysis result, supporting the effectiveness of the appropriate design of this ratio for preventing the oscillatory false triggering.**

***Index Terms*-- Common source inductance; False triggering; Oscillator stability; Power semiconductor devices; FET switches.**

I. INTRODUCTION

The gallium nitride field effect transistors (GaN-FETs) are attracting researchers' attention as a promising next-generation switching device. Owing to their low on-state resistance and fast switching capability [1][2], GaN-FETs are expected to contribute to significant miniaturization and efficiency improvement of the switching power converters. Actually, a number of studies have proven the effectiveness of GaN-FETs for application to ultra-small or extremely high-efficiency power converters [3]–[7].

In contrast to these remarkable features, the GaN-FETs tend to have low gate threshold voltage. As a result, the GaN-FETs have been reported to be susceptible to false triggering [8]–[11], such as the self-turn-on [12], caused by the large switching noise generated as a result of the fast switching.

Particularly, the GaN-FETs have been reported to cause a disastrous trouble called the oscillatory false triggering [13]–[16]. The oscillatory false triggering is a self-sustaining uncontrollable series of repetitive false triggering after a fast switching. In this phenomenon, false turn-ons and false turn-offs repeat at a far higher frequency than the switching frequency. Furthermore, this phenomenon generally lasts far longer period than the switching transient time. As a result, this phenomenon tends to generate enormous switching loss. Therefore, the oscillatory false triggering can be a severe obstacle for industrial application of the GaN-FETs.

The purpose of this paper is to elucidate the design requirement to prevent the oscillatory false triggering. As for the single false triggering without self-sustaining repetition, two factors have been pointed out to play an essential role [17]–[20]: One is the gate-drain capacitance; and the other is the common source inductance [21]–[24], which is the parasitic inductance of the source terminal. Therefore, reducing the gate-drain capacitance and the common source inductance has been known to be effective for preventing single false triggering. However, this simple approach may not be effective for the oscillatory false triggering because the oscillatory false triggering has a different mechanism from the single false triggering.

The preceding studies [13][14] investigated the oscillatory false triggering of GaN-FET and concluded that this phenomenon is caused by the oscillation of the parasitic oscillator formed of the GaN-FET, its parasitic capacitance, and the parasitic inductance of the wiring. According to their theory, the oscillator is excited by the fast voltage and current transience at the switching. The resultant oscillation appears as a self-sustaining repetition of the false triggering, i.e. the oscillatory false triggering. Therefore, their theory implies an effective remedy for preventing the oscillatory false triggering because the oscillation can be avoided by designing the parasitic oscillator to avoid the oscillatory condition.

In fact, [14] investigated the oscillatory condition of this parasitic oscillator under the assumption that the common source inductance is ignorable as a result of eliminating the common source path in the PCB layout. Then, the analysis result revealed that the oscillatory condition is dependent on the resonance frequency of the parasitic resonator in the gating circuit, which is formed of the parasitic inductance of the gate circuit and the gate-source capacitance of the GaN-FET, and

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that of the parasitic resonator in the power circuit, which is formed of the parasitic inductance of the power circuit and the drain-source capacitance. The oscillatory condition was found to be easily satisfied, if these frequencies are close each to the other. In addition, the necessary difference between these frequencies to avoid the oscillation increases as the Q factor of these parasitic resonators become larger. Consequently, this study concluded that the parasitic inductance of the wiring should be designed to separate these frequencies or the resistance should be added in the gating and power circuit to lower the Q factor for avoiding the oscillatory false triggering.

However, these instructions may be difficult to be applied in recent power converters using the GaN-FETs. Recently, the gate resistor is commonly designed to have minimum resistance for extremely high-speed switching. The wirings of the PCBs are also commonly designed to have a minimum length for reducing the parasitic inductance as well as the downsizing of the PCBs. As a result, the gating and power circuits tend to have small parasitic resistance; and the parasitic inductance of these circuits tend to have a similar order of value. Consequently, the parasitic resonators of the gating and power circuits tend to have comparatively large Q factors as well as similar resonance frequencies because the gate-source capacitance and the drain-source capacitance also have the similar order of value in many commercially available switching devices.

As we have seen, the preceding analysis implied difficulty in preventing the oscillatory false triggering in recent power converters of GaN-FETs. However, this result was derived based on the assumption that the common source inductance is ignorable, although this inductance has been pointed out to possibly play an essential role not only in the single false triggering but also in the oscillatory false triggering in a recent study [25]. Therefore, considering the common source inductance may result in another oscillatory condition, possibly leading to another instruction more conveniently applicable to recent power converters using GaN-FETs.

This paper derives a novel design instruction for preventing the oscillatory false triggering through analysis of the parasitic oscillator including the common source inductance. For this purpose, this paper adds the common source inductance to the parasitic oscillator model discussed in the preceding study [14]. Certainly, adding this inductance generally requires complicated analysis to derive the oscillatory false triggering. In order to simplify the discussion, this paper rather neglects the parasitic resistance and the gate resistor.

This corresponds to the worst possible case of the fast switching of the GaN-FETs because these parasitic resonators have infinitely large Q factors and therefore cannot damp their resonance. In fact, the analysis result of the preceding study [14] concluded that this case does not have any possible method to avoid the oscillatory false triggering because the necessary difference in the resonance frequency between the two parasitic resonators becomes infinitely large. Therefore, this worst-case analysis of this paper, ignoring the resistance, reveals the sufficient condition for preventing the oscillatory false triggering, which may be universally applicable to the power converter design.

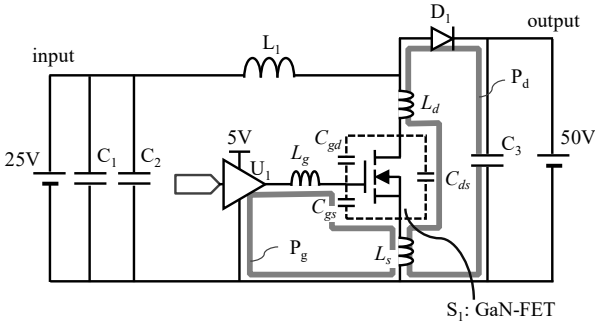
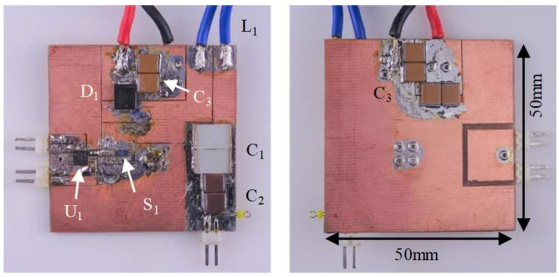


Fig. 1. Circuit diagram of the experiment boost chopper.



(a) Top View (b) Bottom View

Fig. 2. Photographs of the experimental chopper.

TABLE I
SPECIFICATIONS OF THE EXPERIMENTAL CHOPPER

S_1	GaN-FET EPC2010 (EPC Corp.)
D_1	Si-SBD SK4200L (Micro Commercial Components)
C_1	Film capacitor 1nF×2pcs ECWU1105KCV (Panasonic)
C_2	Ceramic capacitor 22uF × 2pcs CKG57NX7S2A226M500JH (TDK Corp.)
C_3	Ceramic capacitor 2.2μF×6pcs CKG57KX7T2E225M335JH (TDK Corp.)
L_1	Inductor 27μH×4pcs 7G14A-270M (Sagami)
U_1	Driver LM5113SDE/NOPB (Texas Instruments)

This paper is the updated version of the conference paper [26], which presented the basic analysis of the oscillatory false triggering. Based on [26], this paper further includes additional experimental evidence that validates the analysis results. In addition, this paper includes more detailed analysis of the oscillatory false triggering, elucidating two different types of the oscillatory false triggering referred to as the Colpitts type and the Hartley type in this paper.

The following discussion consists of 4 sections. Section III briefly reviews the oscillatory false triggering found in an experimental boost chopper. Section IV constructs the analysis model of the parasitic oscillator and elucidates the oscillatory condition to derive the design instructions for the prevention of the oscillatory false triggering. Section V confirms the appropriateness of the analysis result and the resultant design instructions experimentally. Finally, section VI gives conclusions.

II. OSCILLATORY FALSE TRIGGERING

In order to construct an appropriate analytical model of the

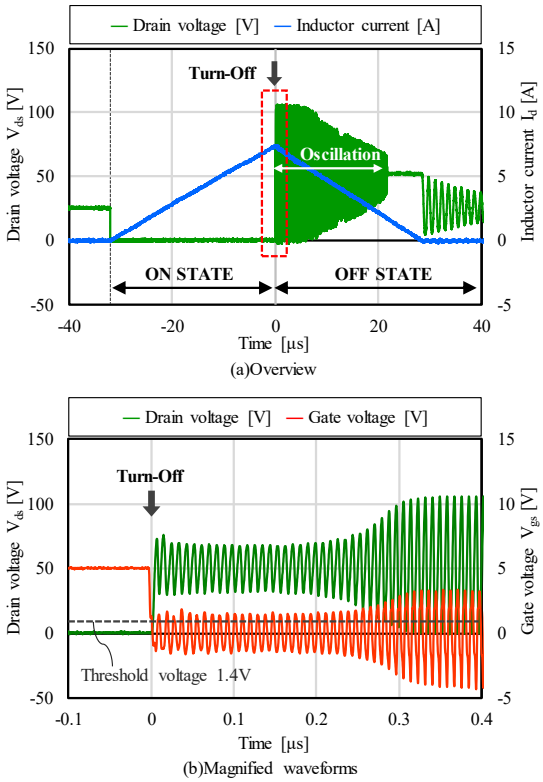


Fig. 3. Experimental waveforms after the turn off.

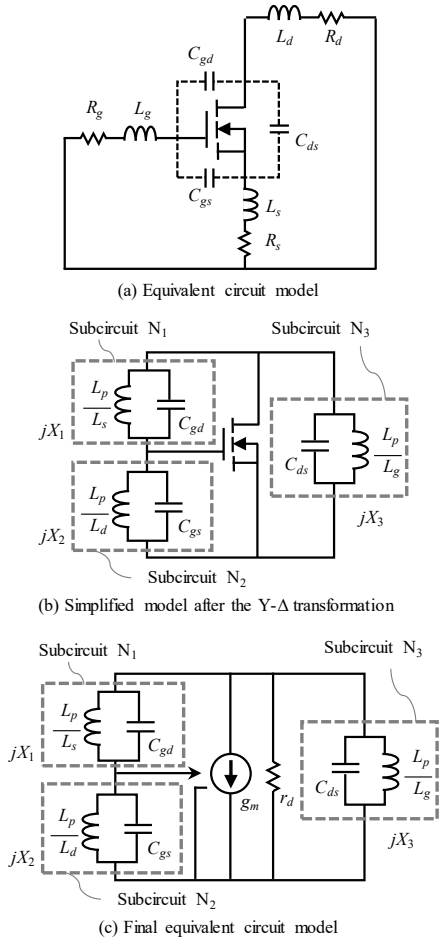


Fig. 4. Analytical models of the oscillatory false triggering.

oscillatory false triggering, this section briefly reviews the basic features of this phenomenon based on the experimental waveforms observed in a boost chopper. Figures 1 and 2 present the circuit diagram and the photographs of the boost chopper, respectively; and Table I shows the list of the circuit elements. This chopper has only one switching device, i.e. GaN-FET S_1, in order to discuss the simplest circuit that causes the oscillatory false triggering. Capacitance C_{gd}, C_{gs}, and C_{ds} are the parasitic capacitance of S_1; L_g and L_d are the parasitic inductance of the loop wiring paths P_g and P_d, respectively; L_s is the common source inductance, which is the inductance of the wiring path shared by P_g and P_d. Parasitic inductance L_g, L_d, L_s are measured as 5.1nH, 8.8nH, and 0.83nH, respectively. The measurement method for the parasitic inductance is presented in the appendix.

The experimental chopper was operated for a single switching cycle to observe the oscillatory false triggering after a single turn-off. For this purpose, the gate voltage of S_1 was first set at 5V to keep S_1 in the on-state for 32μs; and then, the gate voltage of S_1 was set at 0V to observe the oscillatory false triggering after the turn-off.

Figure 3 shows the results. Figure 3(a) shows the high-frequency oscillation in the drain voltage of S_1, which started in coincidence with the turn-off of S_1; and this oscillation lasted for 22μs, which is far longer period than the switching transition time. Figure 3(b) shows the magnified waveform of this oscillation, which appeared in the drain voltage and the gate voltage of S_1. The gate voltage repetitively crossed the gate threshold voltage of 1.4V due to the oscillation. In addition, the drain voltage drops at the rise of the gate voltage. Therefore, this oscillation appears as a series of repetitive false triggering.

The oscillation frequency was found to be 113MHz. This frequency is close to the resonant frequency of the parasitic LC resonator of C_{gs} and L_g, which was calculated as 103MHz based on the capacitance and inductance values, and that of C_{ds} and L_d, which was calculated as 93MHz. Therefore, in this phenomenon, we cannot neglect the parasitic capacitance of S_1 nor the parasitic inductance of the wiring. Furthermore, Fig. 3(b) shows that the amplitude of this oscillation grows after the turn-off of S_1, suggesting that this oscillation is self-sustaining and therefore cannot be explained simply as the parasitic resonance.

These features of the oscillatory false triggering can be reasonably explained as a result of the parasitic oscillator formed of the GaN-FET, the parasitic capacitance, and the parasitic inductance, as discussed in [13][14]. Furthermore, [13][14] elucidated that the oscillatory false triggering can be prevented by designing the parasitic inductance of the wiring not to satisfy the oscillatory condition of this parasitic oscillator. However, this preceding analysis neglected the common source inductance. In the next section, the parasitic oscillator is analyzed considering the common source inductance.

III. Oscillatory Condition of Parasitic Oscillator

A. Model Construction

This subsection constructs the simple analytical model of the parasitic oscillator based on the experimental circuit shown in Fig. 1. In the previous section, the oscillatory false triggering occurred after the turn-off of S_1. In this period, the DC component of the inductor current flowed through the diode D_1. Hence, we simply regard D_1 as the short-circuit. As discussed in the previous section, the oscillatory false triggering has extremely high frequency than the normal switching frequencies of the power converters. Hence, the input and output smoothing capacitors C_1–C_3 are simply approximated as the short-circuit for the modeling of the oscillatory false triggering. On the other hand, the input smoothing inductor L_1 can be approximated as the open-circuit. However, the parasitic capacitance and inductance cannot be neglected to model the parasitic oscillator. As a result, an analytical model of the parasitic oscillator was obtained as Fig. 4(a). The resistance R_g, R_d, and R_s are the parasitic resistance of the wiring paths P_g, P_d, and the common source path, respectively. (R_g includes the gate resistor as well as the internal resistance of the gate terminal of S_1 and the output impedance of the gate driver; R_d includes the equivalent AC resistance of D_1.)

The circuit model of Fig. 4(a) is, however, difficult to directly analyze using the circuit theory. In order to simplify the discussion, this analysis neglects R_g, R_d, and R_s. This corresponds to the worst case, in which the parasitic resonance in the parasitic oscillator model cannot be damped by the resistance. Therefore, the non-oscillatory condition obtained under this approximation is valid also under the existence of R_g, R_d, and R_s, because this analysis reveals a sufficient condition to prevent the oscillatory false triggering.

In addition, the model is further simplified by applying the Y-Δ transformation to the Y-shaped network of L_g, L_d, and L_s. As a result, a simplified equivalent circuit model of the parasitic oscillator is obtained as shown in Fig. 4(b), where L_p is defined as

$$L_p = L_s L_g + L_g L_d + L_d L_s . \tag{1}$$

Next, the switching device S_1 is modeled for the analysis. In this analysis, S_1 is modeled simply as a voltage-controlled current source with the constant mutual conductance g_m and the constant drain-source resistance r_d, which is the simplest model of the field effect transistors. Certainly, the electrical behavior of the switching device generally contains significant non-linearity. However, as we have seen in the previous section, the oscillation in the gate voltage has the same frequency as that in the drain voltage. Therefore, it seems to be natural to suppose that the oscillatory false triggering can be modeled by the linear model, similarly as in [14]. According to the same reason, we simply assume constant C_{gd}, C_{gs}, and C_{ds} regardless of the voltage applied to S_1. These parasitic capacitances are assumed to have the same values as when the DC voltage bias of the experimental condition is applied to S_1. As a result, the analytical equivalent oscillator model is finally obtained as in Fig. 4(c).

B. Oscillatory Condition

Figure 4(c) has the form known as the Barkhausen-type oscillator. The oscillatory condition of this oscillator can be analyzed using the Barkhausen criterion [27]. According to this criterion, the oscillation occurs, if the real part of the open-loop gain H is greater than unity, i.e. $\mathrm{Re}(H)\geq 1$, at the frequency at which the imaginary part of H vanishes, i.e. $\mathrm{Im}(H)=0$.

The open-loop gain H of Fig. 4(c) can be expressed as follows, if the reactance of the parallel LC resonators N_1–N_3 (marked by the dashed lines) are denoted as X_1–X_3, respectively:

$$\begin{aligned} H &= -g_m \{ r_d \,//\, j(X_1 + X_2) \,//\, jX_3 \} \frac{X_2}{X_1 + X_2} \\ &= -\frac{j g_m r_d X_2 X_3}{j(X_1 + X_2) X_3 + r_d (X_1 + X_2 + X_3)}. \end{aligned} \tag{2}$$

Therefore, the Barkhausen criterion can be satisfied, if there is a frequency at which both of the following relations are met.

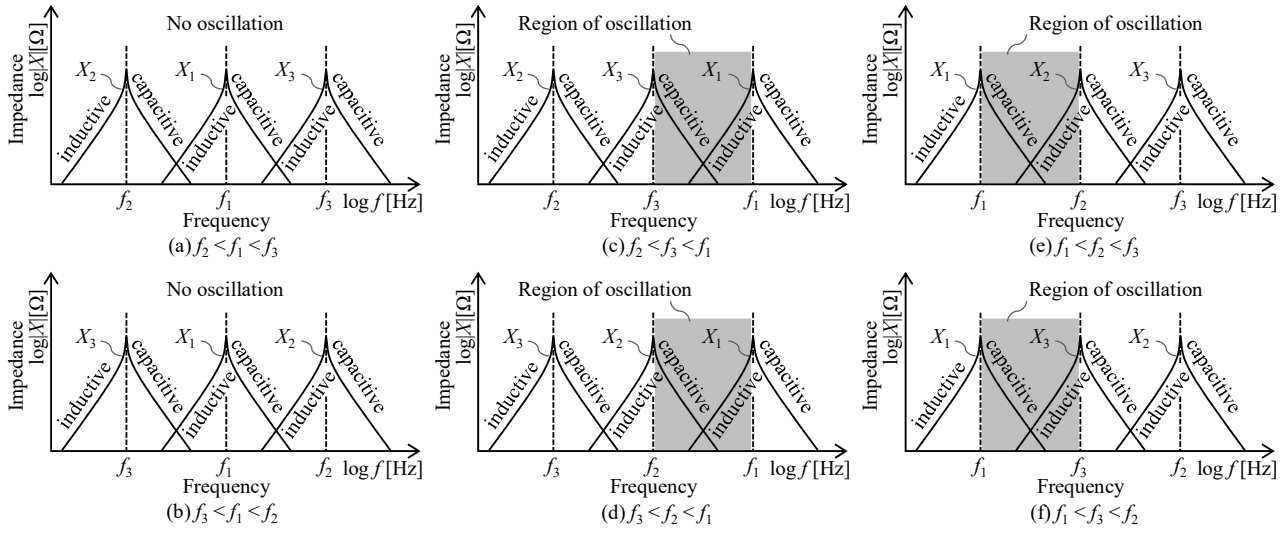


Fig. 5 Frequency region of the oscillation in 6 possible magnitude relation among f_1–f_3. The vertical and horizontal axes are the impedance of N_1-N_3 and the frequency, respectively, both in the logarithmic scale.

$$X_1 + X_2 + X_3 = 0. \tag{3}$$

$$-\frac{g_m r_d X_2}{X_1 + X_2} \geq 1. \tag{4}$$

Equation (3) is called as the frequency condition, whereas (4) is called as the gain condition.

Equation (4) indicates that the oscillation tends to occur at larger probability if the factor $g_m r_d$ takes the larger value. In general, the factor $g_m r_d$ is a finite value depending on the switching device. However, in this analysis, we regard that $g_m r_d$ is infinitely large in order to consider the worst case. Then, the gain condition (4) can be simplified as that X_1+X_2 and X_2 has the opposite polarity. Hence, further considering the frequency condition, the Barkhausen criterion can be simply expressed as follows: the oscillation occurs, if X_1, X_2, and X_3 satisfy either

1. X_2 and X_3 are both positive and X_1 is negative, or
2. X_2 and X_3 are both negative and X_1 is positive,

at the frequency at which X_1+X_2+X_3=0.

The subcircuits N_1–N_3 are the parallel LC oscillators. Hence, the reactance of N_1–N_3 is positive, if the frequency is below the resonance frequency of the subcircuit; and the reactance is negative if the frequency is above the resonance frequency.

If the resonance frequencies of N_1–N_3 are denoted as f_1–f_3, respectively, there are 6 possible magnitude relations among f_1–f_3, as illustrated in Fig. 5. In the 4 relations, i.e. f_2<f_3<f_1, f_1<f_2<f_3, f_3<f_2<f_1, and f_1<f_3<f_2, there is a frequency region in which X_2 and X_3 have the same polarity and X_1 has the different polarity (The shadowed frequency region in Fig. 5.) Note that X_1+X_3 takes an extremely large negative value at the lowest frequency of the shadowed region and an extremely large positive value at the highest frequency in the case of f_2<f_3<f_1 and f_1<f_3<f_2. Therefore, there is a frequency within the shadowed region in which X_1+X_2+X_3=0, indicating that the oscillation, i.e. the oscillatory false triggering, occurs in the case of f_2<f_3<f_1 and f_1<f_3<f_2. Similarly, X_1+X_2 varies from an extremely large negative value to an extremely large positive value within the shadowed region in the case of f_1<f_2<f_3 and f_3<f_2<f_1. Therefore, the oscillatory false triggering also occurs in the case of f_1<f_2<f_3 and f_3<f_2<f_1.

Although all of these 4 relations of f_1–f_3 cause the oscillatory false triggering, the oscillation type of the relations f_2<f_3<f_1 and f_3<f_2<f_1 has a fundamental difference from that of f_1<f_2<f_3 and f_1<f_3<f_2. In f_2<f_3<f_1 and f_3<f_2<f_1, X_1 is inductive in the shadowed region, whereas X_2 and X_3 are both capacitive. Therefore, the oscillation is classified as the Colpitts oscillator. On the other hand, in f_1<f_2<f_3 and f_1<f_3<f_2, X_1 is capacitive in the shadowed region, whereas X_2 and X_3 are inductive. Therefore, the oscillation is classified as the Hartley oscillator. Regarding this difference in the oscillation type, there is also a difference in the oscillation frequency. As can be seen in Fig. 5, the oscillation frequency is higher than f_2 and f_3 in the Colpitts type oscillation. On the other hand, the oscillation frequency is lower than f_2 and f_3 in the Hartley type oscillation. (Hereafter, we distinguish these types in the oscillatory false triggering as the Colpitts-type oscillatory false triggering and the Hartley-type oscillatory false triggering.)

Noting that f_1–f_3 can be expressed as

$$f_1 = \frac{1}{2\pi\sqrt{L_p C_{gd}/L_s}}, \quad f_2 = \frac{1}{2\pi\sqrt{L_p C_{gs}/L_d}}, \quad f_3 = \frac{1}{2\pi\sqrt{L_p C_{ds}/L_g}}, \tag{5}$$

the condition of the Colpitts type oscillatory false triggering can be expressed as

$$\frac{L_d}{C_{gs}} < \frac{L_g}{C_{ds}} < \frac{L_s}{C_{gd}} \quad \text{or} \quad \frac{L_g}{C_{ds}} < \frac{L_d}{C_{gs}} < \frac{L_s}{C_{gd}}, \tag{6}$$

whereas the condition of the Hartley type oscillatory false triggering can be expressed as

$$\frac{L_s}{C_{gd}} < \frac{L_d}{C_{gs}} < \frac{L_g}{C_{ds}} \quad \text{or} \quad \frac{L_s}{C_{gd}} < \frac{L_g}{C_{ds}} < \frac{L_d}{C_{gs}}. \tag{7}$$

Contrary to the aforementioned 4 relations of f_1–f_3, the remaining two magnitude relations of f_1–f_3, i.e. f_2<f_1<f_3 and f_3<f_1<f_2, do not have the frequency region in which X_2 and X_3 have the same polarity and X_1 has the different polarity. Therefore, the oscillatory false triggering does not occur in these cases. According to (5), the condition for preventing the oscillatory false triggering, i.e. f_2<f_1<f_3 and f_3<f_1<f_2, can be rewritten as

$$\frac{L_d}{C_{gs}} < \frac{L_s}{C_{gd}} < \frac{L_g}{C_{ds}} \quad \text{or} \quad \frac{L_g}{C_{ds}} < \frac{L_s}{C_{gd}} < \frac{L_d}{C_{gs}}. \tag{8}$$

Equation (8) indicates that the ratio L_s/C_{gd} should be designed between L_d/C_{gs} and L_g/C_{ds}. This fact implies a striking idea that too small L_s, as well as too large L_s, can cause the oscillatory false triggering. Consequently, this result suggests a novel design instruction that the appropriate balance between L_s and C_{gd}, i.e. the appropriate ratio of L_s to C_{gd}, should be designed to satisfy (7) in order to prevent the oscillatory false triggering.

Compared with the conventional design instruction [14], this design instruction can suppress the oscillatory false triggering, even if the parasitic resonance frequency of the gating circuit is close to that of the power circuit, as shown below.

According to [14], the parasitic resonance frequency of the gating circuit (f_g) and that of the power circuit (f_d) can be expressed as follows, if C_{gd} is approximated to be far smaller than C_{gs} and C_{ds}.

$$f_g = \frac{1}{2\pi\sqrt{(L_g + L_s)C_{gs}}}, \quad f_d = \frac{1}{2\pi\sqrt{(L_d + L_s)C_{ds}}}. \tag{9}$$

Therefore, if L_s is approximated to be far smaller than L_g and L_d, i.e. L_g+L_s≈L_g and L_d+L_s≈L_d, (8) can be rewritten as

$$\frac{1}{4\pi^2 C_{ds} C_{gs}} \frac{1}{f_d^2} < \frac{L_s}{C_{gd}} < \frac{1}{4\pi^2 C_{ds} C_{gs}} \frac{1}{f_g^2} \quad \text{or} \quad \frac{1}{4\pi^2 C_{ds} C_{gs}} \frac{1}{f_g^2} < \frac{L_s}{C_{gd}} < \frac{1}{4\pi^2 C_{ds} C_{gs}} \frac{1}{f_d^2}. \tag{10}$$

As can be seen in (8), the occurrence condition of the oscillatory false triggering can be prevented as far as the ratio of L_s and C_{gd} is designed within the appropriate range. Certainly, this range tends to be narrow, if f_g and f_d are close. However, designing the ratio L_s/C_{gd} to satisfy (10) can be a universal approach for preventing the oscillatory false triggering. Noting

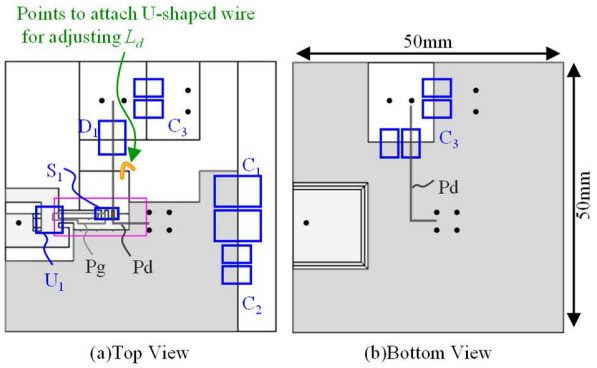


Fig. 6. Pattern layout of the experimental PCB.

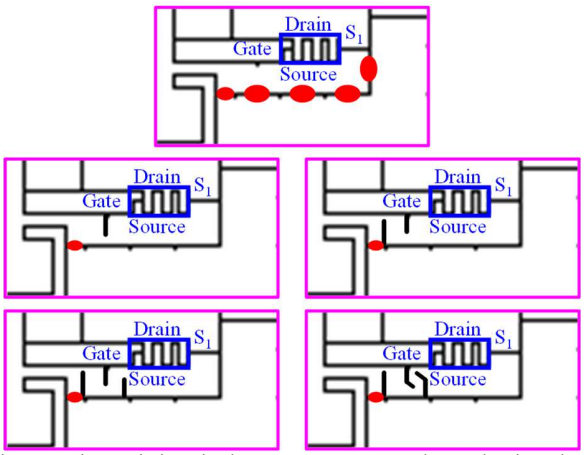


Fig. 7. Nine variations in the common source paths. Red points show the points for making a solder bridge.

that L_s can be varied by small change in the PCB layout at the source terminal, (10) may be interpret as the necessity of the appropriate design of L_s in accordance with C_{gd}, which is specified by the datasheet of the switching device, in order to achieve the fast switching without the oscillatory false triggering.

It is worth noticing that this analysis is based on the worst case, in which the parasitic resistance including the gate resistance is regarded to be zero and $g_m r_d$ is infinitely large. Therefore, this design instruction can be supposed to cover extremely high-speed switching.

Certainly, actual power converters have the gate resistance and the parasitic resistance of the wiring; and the switching devices have a finite value for $g_m r_d$. Therefore, these parasitic resistances may damp the oscillation; and the gain condition (4) may not be satisfied due to the limited value of $g_m r_d$. As a result, the oscillatory condition may be prevented in the wider region of L_s/C_{gd} in actual power converters. (In other words, the condition of (8) or (10) can be interpreted as a sufficient condition for preventing the oscillatory false triggering.)

Fig. 8. Photograph of the U-shaped wires.

As discussed above, the ratio between L_s and C_{gd} should have an appropriate range of value to satisfy (8) or (10). However, this does not necessarily deny the effort to minimize L_s and C_{gd}. As widely known, large C_{gd} or L_s may deteriorate the switching speed or cause the self-turn-on. Therefore, the proposed design instruction should be interpreted as that reduction merely in C_{gd} or in L_s may be hazardous and that both of C_{gd} and L_s should be reduced to keep L_s/C_{gd} within an appropriate range.

IV. Experiment

An experiment was carried out to verify the proposed design instruction as well as the analysis results of the oscillatory false triggering. For this purpose, the occurrence of the oscillatory false triggering was observed at various ratios of L_s and C_{gd}.

This experiment utilized the experimental chopper shown in Section II. Figure 6 shows the PCB layout of the experimental chopper. The PCB layout was designed to be able to have a variation in the common source path, i.e. the current path shared by P_g and P_d defined in Fig. 1. The common source path was varied by selecting a point to make a solder bridge to connect the ground of the power circuit to the source terminal of S_1 as well as adding a small cut in the pattern of the common source path. As a result, nine types of the common source path were implemented as shown in Fig. 7; and L_s was ranged from 0.32nH to 2.11nH, as listed in Table II. The common source inductance L_s was measured using the recently proposed technique [23][24]. A brief review of this method is presented in the appendix.

In addition, C_{gd} was also varied by adding a small-sized ceramic capacitor between the drain and gate terminals of S_1. As a result, 7 levels in C_{gd} was implemented: 9.2pF, 14pF, 21pF, 27pF, 31pF, 36pF, and 42pF. (The first value is the original C_{gd} of S_1.)

Changing the common source path for making a variation in

TABLE II
Inductance Values of L_s, L_g and L_d Employed in the Experiment

L_s [nH]	0.32	0.38	0.56	0.83	1.21	1.28	1.49	1.64	2.11
L_g [nH]	5.2	5.2	5.2	5.1	5.2	5.3	5.4	5.4	5.6
Length of the U-shaped wire [mm]	10	10	5	5	0	0	0	0	0
L_d [nH]	8.5	8.8	7.9	8.8	8.1	8.2	8.6	8.8	8.8

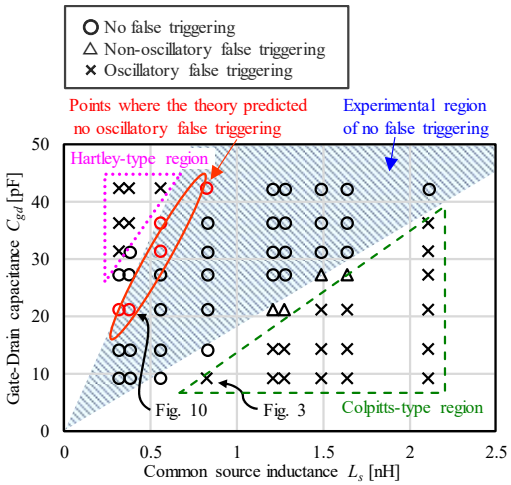


Fig. 9. Experimental result of occurrence of the oscillatory false triggering. Red marks indicate the points where the theory predicted non-occurrence of the oscillatory false triggering.

L_s also slightly affected the wiring path length for P_d. In order to adjust L_d at a constant value, one of two types of U-shaped wires was inserted to elongate the drain wiring path for some levels of L_s. The photograph of the U-shaped wires is shown in Fig. 8. As a result, both of L_g and L_d were kept at almost constant values regardless of the variation in L_s, as listed in Table II. The measurement method for L_g and L_d are also described in the appendix.

In order to evaluate the effectiveness of the proposed design instruction, L_g and L_d were designed so that the parasitic resonance frequency f_g were close to f_d. (Definition of f_g and f_d are given in (9).) As shown later, this design caused the oscillatory false triggering at the extremely low value of L_s and comparatively large C_{gd}, indicating that the conventional design instruction is not satisfied.

We set L_s and C_{gd} at various values and observed the occurrence of the oscillatory false triggering to evaluate the dependence of the oscillatory false triggering on the ratio between L_s and C_{gd}. The method to observe the oscillatory false triggering is the same as section II. At first, we kept S_1 in the on-state for 32μs. Then, S_1 is turned off at the inductor current of 7.4A; and the drain and gate voltage were observed after the switching.

Figure 9 shows the experimental result. In this figure, the repetitive false triggering more than ten times after the turn off was judged as the oscillatory false triggering. The false triggering less than ten times was denoted as the non-oscillatory false triggering.

As can be seen in Fig. 9, the oscillatory false triggering was suppressed in a certain range of L_s/C_{gd}. Excessively large L_s/C_{gd}, as well as excessively small L_s/C_{gd}, resulted in the oscillatory false triggering, as is expected by the theoretical analysis. Therefore, this result implies that balancing L_s and C_{gd} is essential for preventing the oscillatory false triggering rather than simply minimizing either L_s or C_{gd}.

The points where the theory predicted no oscillatory false triggering are marked in the red color in Fig. 9. The experimental region without the oscillatory false triggering

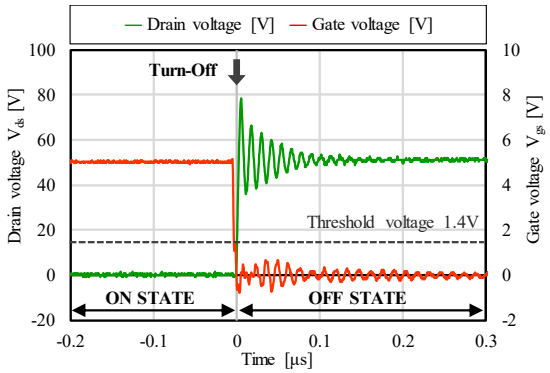


Fig. 10. Voltage waveforms at the turn-off when the oscillatory false triggering does not occur.

entirely covered the theoretically predicted region, as is consistent with the fact that the theory gives the sufficient condition for preventing the oscillatory false triggering. Consequently, this result supported that the appropriate balance between L_s and C_{gd} can prevent the oscillatory false triggering.

Figure 10 shows the switching waveforms when the oscillatory false triggering was suppressed by setting L_s at 0.38nH and C_{gd} at 21pF, respectively. (L_g and L_d were 5.2nH and 8.8nH, respectively.) As can be seen in this figure, the gate voltage remains below the threshold voltage of 1.4V after the turn-off. Therefore, not only the oscillatory false triggering but also the normal oscillatory false triggering disappeared in the switching waveform, suggesting the practical effectiveness of the proposed design instruction.

In order to further verify the theoretical analysis, we investigated the gate and drain voltage waveforms of the oscillatory false triggering. As discussed in the previous section, the theory predicted two types of the oscillatory false triggering: The Colpitts-type and Hartley-type oscillatory false triggering. The Colpitts-type is predicted to occur at large L_s/C_{gd} and to have higher oscillation frequency than f_2 and f_3, whereas the Hartley type is predicted to occur at small L_s/C_{gd} and to have lower oscillation frequency than f_2 and f_3. Therefore, we measured the oscillation frequency of the region of large L_s/C_{gd} (surrounded by the green dashed line), which corresponds to the Colpitts-type region, and the region of small L_s/C_{gd} (surrounded by the pink dotted line), which corresponds to the Hartley-type region. Then, we compared the oscillation frequency with f_2 and f_3, which are calculated based on (5).

Table III shows the result. In all the points in which the oscillatory false triggering occurred, the oscillation frequency was found to be higher than f_2 and f_3 in the Colpitts-type region, whereas the oscillation frequency was lower in the Hartley-type region.

In addition to the oscillation frequency, the phase of the oscillation waveforms in the gate and drain voltage was also evaluated in all the points of the oscillatory false triggering. As shown in the appendix, the phase difference of the gate voltage from the drain voltage should be slightly greater than 180° in the Colpitts-type, whereas the phase difference should be slightly smaller than 180° in the Hartley-type. Therefore, we compared the phase difference observed in the experimental

TABLE III
OSCILLATION FREQUENCY AND PHASE DIFFERENCE BETWEEN GATE AND DRAIN VOLTAGE OSCILLATION

Type of the oscillatory false triggering	f_2 [MHz]	f_3 [MHz]	Oscillation frequency [MHz]	Phase angle of v_g/v_d [°]
Colpitts-type	91.3	83.3	113	184
	86.5	82.8	120	194
	86.5	82.8	119	197
	85.2	81.8	119	197
	85.2	81.8	118	195
	82.9	78.5	140	224
	82.9	78.5	118	194
	82.9	78.5	118	188
	81.8	76.5	146	239
	81.8	76.5	133	190
	81.8	76.5	118	190
	77.1	73.5	172	236
	77.1	73.5	167	225
	77.1	73.5	150	326
	77.1	73.5	120	193
	77.1	73.5	119	212
	77.1	73.5	112	190
Hartley-type	97.0	90.6	70.8	82
	97.0	90.6	68.8	100
	97.0	90.6	67.0	126
	96.3	88.4	70.0	123
	96.3	88.4	67.0	117
	93.7	90.8	75.0	86

waveforms between the Colpitts-type region and the Hartley type region.

The result is also presented in Table III. The points of the Colpitts-type region showed larger phase differences than 180°, whereas the points of the Hartley type region showed smaller phase differences than 180°, as is expected from the theory. Consequently, both of the oscillation frequency and the phase difference were found to be consistent with the difference between the Colpitts-type oscillatory false triggering and the Hartley-type oscillatory false triggering, supporting the appropriateness of the theoretical analysis in Section III.

V. CONCLUSIONS

The oscillatory false triggering has been reported to be a possible risk for industrial application of GaN-FETs. This paper addressed this issue by proposing a novel design instruction to prevent this phenomenon. The occurrence condition of the oscillatory false triggering was analyzed, considering the common source inductance as well as the other parasitic inductance of the wiring. As a result, the ratio of the common source inductance to the gate-drain capacitance was elucidated to be a key factor for effective prevention of the oscillatory false triggering. The analysis revealed that too small common source inductance can be harmful as too large common source inductance, suggesting the necessity to optimize the common source inductance in accordance with the gate-drain capacitance.

APPENDIX

A. Measurement Method of Common Source Inductance L_s

A recently proposed technique [23][24] was employed for the common source inductance measurement. Figure 11 illustrates the measurement method. This method employs another PCB with the same layout pattern as the experimental chopper. On this PCB, only the GaN-FET was mounted. Next, a resistor R_{mesu} with sufficiently large resistance was attached on the wiring path from the gate driver to the gate terminal of the GaN-FET. In addition, ceramic capacitor C_{mesu} with far larger capacitance than the gate-source parasitic capacitance of the GaN-FET was attached to connect the pads for the output terminal and the ground terminal of the gate driver. Then, we applied the DC voltage to C_{mesu} in order to keep the GaN-FET at the on-state. Finally, we connected the signal generator between the drain and the source of the GaN-FET to supply the high-frequency sinusoidal AC current and measured the AC voltage across R_{mesu}.

As discussed in the preceding studies [23][24], the voltage induced at L_s appears at R_{mesu} because the resistance of R_{mesu} was designed to be far higher than the impedance of C_{gs}, C_{mesu}, and L_g at the frequency of the sinusoidal AC current. Hence, L_s can be obtained using the following equation:

$$L_s = \frac{V_{mesu}}{2\pi f I_{ac}} \sin\phi, \tag{11}$$

where V_{mesu} and I_{ac} are the effective value of the voltage across R_{mesu} and the AC current supplied from the signal generator,

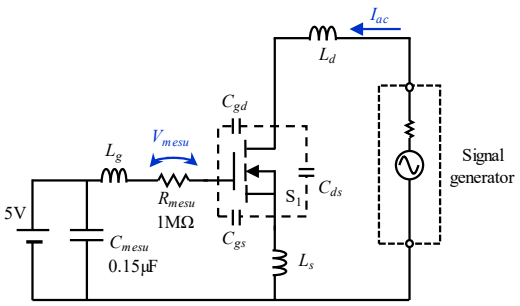


Fig. 11. Circuit diagram of the common source inductance measurement system.

respectively; f is the frequency of the AC current; and ϕ is the phase difference between the voltage across R_{mesu} and the AC current.

We measured L_s by supplying the AC current of 0.2–0.3Ap at eleven frequencies in the range from 2MHz to 12MHz. Then, we averaged the results to determine L_s. Other parameters related to this measurement is presented in Fig. 11.

B. Measurement Method of Parasitic Inductance L_g and L_d

The inductance L_g and L_d are measured using the simple measurement method for the parasitic inductance of the loop wiring path [14]. In this method, another PCB with the same layout pattern as the experimental chopper is employed, similarly as in the previous subsection.

For the measurement of L_g, only a small surface-mount ceramic capacitor C_{mg} was mounted on the pads for the GaN-FET to connect the gate and source terminals. In addition, we made a solder bridge to connect the pads of the output and ground terminals of the gate driver. As a result, C_{mg} was short-circuited through the wiring of the gating circuit.

Then, we measured the frequency dependence of the impedance of this short-circuited capacitor. This short-circuited capacitor forms a parallel-connected LC resonator composed of the ceramic capacitor and the parasitic inductance L_g+L_s. Therefore, the resonance frequency can be measured based on the frequency at the peak impedance. If we denote the resonance frequency as f_{res}, L_g can be obtained as

$$L_g = \frac{1}{4\pi^2 f_{res}^2 C_{mg}} - L_s. \tag{12}$$

On the other hand, for the measurement of L_d, we mounted only a small surface-mount ceramic capacitor C_{md} on the pads for the GaN-FET to connect the drain and source terminals. Then, we made solder bridges to short the pads for the two terminals of diode D_1 as well as the two terminals of output capacitor C_3. As a result, C_{md} was short-circuited through the wiring of the power circuit. This short-circuited capacitor forms a parallel-connected LC resonator composed of the ceramic capacitor and the parasitic inductance L_d+L_s. Hence, by determining the resonance frequency by the impedance measurement, we can obtain L_d as

$$L_d = \frac{1}{4\pi^2 f_{res}^2 C_{md}} - L_s. \tag{13}$$

In this experiment, we set both C_{mg} and C_{md} at 0.22uF.

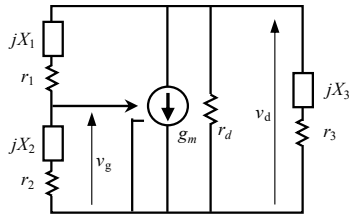


Fig. 12. Oscillator model including parasitic resistance.

C. Phase Difference in Colpitts and Hartley Oscillator

The idealized analysis in Section III neglected the parasitic resistance to simplify the discussion. However, in the actual oscillators, the oscillator model, shown in Fig. 12, has not only the reactance X_1–X_3 but also small resistance r_1–r_3, which makes the phase difference between the gate voltage oscillation and the drain voltage oscillation.

Let v_g and v_d be the voltage oscillation at the gate terminal and the drain terminal of the GaN-FET, respectively. Then, the transfer function from v_d to v_g can be formulated as

$$\begin{aligned}\frac{v_g}{v_d} &= \frac{r_2 + jX_2}{(r_1 + r_2) + j(X_1 + X_2)} \\ &= \frac{r_2(r_1 + r_2) + X_2(X_1 + X_2)}{(r_1 + r_2)^2 + (X_1 + X_2)^2} \\ &\quad + j\frac{X_2(r_1 + r_2) - r_2(X_1 + X_2)}{(r_1 + r_2)^2 + (X_1 + X_2)^2}.\end{aligned} \tag{14}$$

We assume that the resistance r_1–r_3 are far smaller than X_1–X_3; and therefore, we assume that r_1–r_3 do not significantly affect the Barkhausen conditions (3) and (4). Hence, when the oscillatory false triggering occurs, we have

$$\begin{aligned}&r_2(r_1 + r_2) + X_2(X_1 + X_2) \cong X_2(X_1 + X_2) < 0, \\ &\operatorname{sgn}\{X_2(r_1 + r_2) - r_2(X_1 + X_2)\} = \operatorname{sgn}(X_2).\end{aligned} \tag{15}$$

The order of the real part of v_g/v_d is greater than the imaginary part of v_g/v_d. Consequently, v_g/v_d of the Colpitts oscillator has the phase angle slightly greater than 180° due to their negative X_2, whereas v_g/v_d of the Hartley oscillator has the phase angle slightly smaller than 180°.

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