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Straightforward Measurement Method of Common Source Inductance for Fast Switching Semiconductor Devices Mounted On-board

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***Abstract*—Recent progress of wide-bandgap semiconductor switching devices enabled extremely high frequency operation of power converters owing to their ultra-fast switching capability. Fast switching may cause large switching noise at the common source inductance, which may increase the switching loss and lead to false triggering. Therefore, measurement of the common source inductance is often intensely required in practical design of fast switching power converters. However, measurement of the common source inductance is difficult, because 1. the wiring path hidden beneath the molded package significantly contributes to this inductance, 2. the mutual inductance between the gating circuit and the power circuit also contributes to this inductance, and 3. this inductance cannot be defined as the stray inductance of a loop wiring path. These difficulties are addressed in this paper by proposing a novel measurement method of the common source inductance. The proposed method is applicable to already-mounted power circuits. In addition, the proposed method offers a straightforward measurement procedure with common instruments, such as a signal generator, an oscilloscope, voltage and current probes. Along with the measurement principle, this paper also presents an experiment to evaluate the proposed method.**

***Index Terms*— Common Source Inductance, Inductance measurement, Semiconductor package, Stray Inductance.**

I. Introduction

RECENTLY, wide bandgap semiconductor devices, such as SiC-MOSFETs [1]–[3] and GaN-HEMTs [4][5], are emerging as promising switching devices for further miniaturization and efficiency improvement of power converters. These devices are reported to show lower on-resistance and faster switching capability compared with conventional Si-based switching devices. Owing to their fast switching capability, the switching frequency can be increased to reduce the necessary inductance or capacitance of passive components, thus contributing to miniaturization of power converters. In addition, their low on-resistance can reduce the conduction loss at the switching devices, thus contributing to the efficiency improvement.

However, practical design of fast switching power converters requires detailed layout design of PCBs or busbars, as well as appropriate selection of the packages of the switching devices. As widely known, fast switching may cause large switching noise because sudden change in the current across the switching device can induce large voltage due to the stray inductance of the power circuit.

For example, the stray inductance of the half-bridge circuit, as well as the equivalent series inductance of the smoothing capacitors connected to the half-bridge circuit, is reported to cause the switching surge in the drain voltage [6]–[9]. In addition, the stray inductance contributed by the ground line of the power circuit is known to cause the common-mode noise induced by the switching [10]–[12].

Beside of the above-mentioned stray inductance of the power circuit, the common source inductance can also affect the performance of the power converter. This inductance is the stray inductance of the common source path, which is the wiring path shared by the power circuit and the gating circuit. Certainly, this inductance is commonly far smaller than the stray inductance of the power circuit. However, this inductance can increase the switching loss by deteriorating the switching speed, as reported in literature [6], [13]–[20]. In addition, this inductance can cause spurious oscillation in the gate voltage leading to the false triggering [21][22].

The stray inductance is generally dependent on the layout of PCBs or busbars. Furthermore, the wiring hidden beneath the mold of the semiconductor package can affect the stray inductance. Therefore, practical measurement method of the stray inductance of the layout and the package is essential for designing fast switching converters.

In many cases, measurement of the stray inductance is more difficult than that of the inductance of magnetic components, such as inductors or transformers, because the stray inductance is generally far smaller than that of probes for the measurement

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instrument. In spite of this difficulty, a number of techniques have been proposed for measurement of the stray inductance of the power circuit.

For example, impedance analyzers or network analyzers with special probes have been employed to measure the stray inductance of wiring paths [23]–[25]. In this method, careful calibration is required to eliminate the effect of the stray inductance of the probe from the measurement result. Besides, TDR method has been proven to be effective for measuring the stray inductance of wiring paths forming a ladder-type network [26]–[28]. In addition, a concise method that measures the parasitic LC resonance of a wiring path is employed in [29][30] to measure the total stray inductance of loop wiring paths formed in the power circuit.

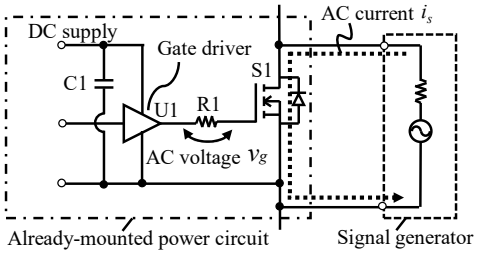
However, as for measurement of the common source inductance, these methods may be difficult to be applied because of the following three features of this inductance.

1) The voltage induced at the common source inductance is difficult to be directly measured because the voltage of the source on the semiconductor chip is generally hidden beneath the mold of the semiconductor package.
2) The common source inductance is not necessarily a lumped inductance disposed on the common source path. Actually, the mutual inductance between the gating circuit and the power circuit can appear as the equivalent common source inductance [14], as shown the appendix.
3) The common source inductance cannot be defined as the stray inductance of a loop wiring path.

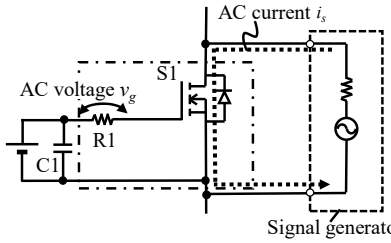
Feature 1 implies difficulty of the measurement method with impedance analyzers or network analyzers because this method requires connecting the source on the chip to the measurement instrument. In addition, feature 2 implies difficulty of the TDR method because the TDR method supposes that the wiring path to be tested can be expressed as a circuit network of inductance or capacitance. Finally, feature 3 also implies difficulty of the resonance method because this method requires that the wiring path to be tested should form a loop.

As can be seen above, these conventional methods may have difficulties in precise measurement of the common source inductance. Certainly, simulation has been widely utilized for estimating the common source inductance [13], [19], [31]–[37]. However, the simulation generally needs information of the physical wiring structure hidden in the mold of the semiconductor package. Therefore, the simulation may be inconvenient for many circuit engineers except for manufacturers of the switching device under test.

The purpose of this paper is to propose a simple measurement method of the common source inductance. The proposed method can avoid difficulties related to the aforementioned three features. Besides, the proposed method is directly applicable to switching devices of already-mounted practical power circuits. This advantage is important because not only the semiconductor package as well as the layout of the PCB or busbar affects the common source inductance. In addition, the proposed method offers a straightforward measurement procedure with common instruments for electronics engineers, such as a signal generator, an oscilloscope, a voltage probe, and a current probe.



(a) A case in which a switching device and a gate driver is mounted



(b) A case in which only a switching device is mounted

Fig. 1. Schematic diagram of the proposed method applied to a switching device under test.

The following discussion consists of 3 sections. Section II describes the proposed method. This section explains how the proposed method can avoid difficulties caused by the aforementioned three features. In addition, this section also presents the reason why the proposed method is directly applicable to a switching device of an already-mounted power circuit. Then, section III presents the experiment to evaluate the proposed method. Finally, section IV gives conclusions.

II. Proposed Measurement Method

A. Overview

This subsection presents the basic procedure of the proposed measurement method of the common source inductance. The proposed method can be applicable to a semiconductor switching device mounted on-board.

Fig. 1 illustrates the proposed method applied to a semiconductor switching device under test. Fig. 1(a) is a basic case in which a gate driver is mounted along with the switching device. Resistor R1 is a resistor with extremely large resistance mounted in replace of the gate resistor. (The required resistance value is discussed later.) Capacitor C1 is the decoupling capacitor for the power supply to the gate driver. The gate driver in Fig. 1(a) is assumed to output the GND level voltage during the off-state of S1. However, the same measurement procedure is also applicable, even if the gate driver outputs a negative voltage during the off-state of S1.

The proposed method consists of the following four steps:

1) Replace the gate resistor by R1.
2) Operate the gate driver U1 to keep the output voltage at the HIGH level. In other words, S1 is kept at the on-state.
3) Connect a signal generator between the drain terminal and the source terminal to supply AC current. In this paper, the AC current has a frequency higher than 1MHz.

4) Measure the AC current supplied from the signal generator as well as the AC voltage induced across R1. Then, the common source inductance L_s can be obtained as

$$L_s = \frac{v_g}{\omega i_s}\sin\phi, \tag{1}$$

where i_s and v_g are the RMS values of the AC current and voltage, respectively; ω is the angular frequency of the AC current, and ϕ is the phase difference between the measured AC voltage and current.

The proposed measurement method is also applicable, even if neither a gate driver nor a gate resistor is mounted. In this case, steps 1 and 2 should be replaced by the following instructions: Connect a parallel-connection of a DC voltage source and a decoupling capacitor C1 between the gate and source terminals of S1 via a resistor with extremely large resistance (R1); then, supply a sufficient voltage that keeps S1 at the on-state. Therefore, the proposed method can be illustrated as Fig. 1(b). If S1 is mounted on a PCB with the pattern for the gating circuit, R1 should be mounted directly on the PCB pads for the gating resistor. In addition, C1 should be mounted directly on the PCB pads of the output and GND terminals of U1, whereas the DC voltage source can be connected from outside the PCB. This can form the same wiring path as the actual gating circuit to suppress the measurement error because the layout of the gating circuit can affect the common source inductance as shown in the appendix.

B. Measurement Principle

As discussed in the appendix, the mutual inductance between the drain current path, i.e. the current path of the drain current flowing from the drain terminal to the source terminal, and the wiring path of the gating circuit, i.e. the wiring path that connects the source terminal to the gate terminal, appears as the equivalent common source inductance. It is worth noting that this equivalent common source inductance caused by the mutual inductance cannot be distinguished from the self-inductance of the common source path by the measurement of the electric behavior. Therefore, from the practical viewpoint of the electric behavior, this equivalent common source inductance can be regarded as a part of the common source inductance as well as the self-inductance of the common source path. Hereafter, this paper treats the common source inductance as is including the equivalent common source inductance.

The fact that the mutual inductance cannot be distinguished from the other constituents of the common source inductance further implies another possibility of interpretation of the common source inductance. In fact, the common source inductance may be rather regarded entirely as the mutual inductance between the drain current path and the wiring path of the gating circuit from the viewpoint of the electric behavior.

This interpretation is convenient because the well-known measurement method of the mutual inductance can be applied to measurement of the common source inductance. As for mutual inductance measurement of a transformer, the AC current is applied to the primary winding, while the secondary

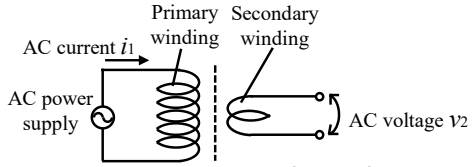


Fig. 2. Mutual inductance measurement of a transformer.

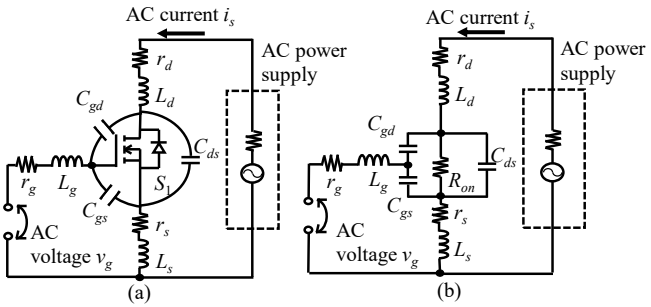


Fig. 3. AC equivalent circuit model of the mutual inductance measurement method applied to the common source inductance.

wiring is kept open, as shown in Fig. 2. Then, the AC current of the primary winding, as well as the induced AC voltage in the secondary winding, is measured. If the RMS values of these AC current and voltage are denoted as i_1 and v_2, respectively, the mutual inductance M can be obtained as

$$M = \frac{v_2}{\omega_M i_1}\sin\phi_M, \tag{2}$$

where ω_M is the angular frequency of the AC current, and ϕ_M is the phase difference between the measured AC voltage and current.

In application of this method to measurement of the common source inductance, the drain current path corresponds to the primary winding. In addition, the wiring path of the gating circuit corresponds to the secondary winding. Next discussion briefly shows how this approach can determine the common source inductance using a simple AC equivalent circuit model. Detailed derivation of this model is discussed in the appendix.

Fig. 3(a) shows the AC equivalent circuit model of the semiconductor switching device under test (S1). Switch S1 is assumed to be mounted on a PCB with the pattern for the gating circuit, whereas no circuit element is assumed to be mounted except for S1. Capacitance C_{ds}, C_{gs}, and C_{gd} are the parasitic capacitance of the device. Resistance r_d, r_g, and r_s are the parasitic resistance of the wiring. Inductance L_d and L_g are the equivalent stray inductance of the power circuit and the gating circuit, respectively, whereas L_s is the common source inductance, i.e. the equivalent stray inductance of the common source path. (The equivalent stray inductance and the parasitic resistance of the source and drain wirings are integrated into L_d and r_d.) Inductance L_d, L_g, and L_s are not identical to the self-inductance of the wirings. However, they contain the mutual inductance as shown in the appendix.

Switch S1 is assumed to be kept at the on-state. In addition, the wiring path between the gate and source terminals are assumed to be opened. Therefore, S1 can be regarded as the on-resistance R_{on} with the stray capacitance. As a result, Fig.

3(a) can be equivalently expressed as Fig. 3(b).

Then, AC current is applied between the drain and source terminals. The current induces the voltage across L_s, r_s, R_{on}, C_{gs}, C_{gd}, and C_{ds}. On the other hand, L_g, and r_g have no voltage drop because no AC current flows through the gate terminal. Therefore, the AC voltage between the gate and source terminals, i.e. v_g in Fig. 3(b), can be expressed as

$$v_g = \left(r_s + j\omega L_s\right)i_s + \frac{\alpha R_{on}}{j\omega C_{par} R_{on} + 1} i_s, \tag{3}$$

where C_{par} is defined as $C_{par}=C_{ds}+C_{gs}C_{gd}/(C_{gs}+C_{gd})$ and α is defined as $\alpha=C_{gd}/(C_{gs}+C_{gd})$.

Now, the angular frequency ω is assumed to be chosen so that $R_{on} << 1/\omega C_{par}$. In this case, (3) can be approximated as

$$v_g \approx \left(r_s + \alpha R_{on}\right)i_s + j\omega\left(L_s - \alpha R_{on}^2 C_{par}\right)i_s. \tag{4}$$

Note that C_{par} has at most the order of nF and R_{on} has at most the order of tens of mΩ in many switching devices. In addition, C_{gd} is far smaller than C_{gs} in general. On the other hand, as shown later in the experiment, the common source inductance tends to have the order of nH. Therefore, $\alpha R_{on}^2 C_{par}$ can be generally neglected compared with L_s. (Note that $\alpha R_{on}^2 C_{par}$ has the dimension of the inductance.) As a result, v_g can be further approximated as

$$v_g \approx \left\{\left(r_s + \alpha R_{on}\right) + j\omega L_s\right\}i_s. \tag{5}$$

Equation (5) indicates that the common source inductance can be obtained according to (1).

As can be seen above, this approach requires applying AC current to S1, while the wiring path between the gate and source terminals is opened. However, this requirement cannot be literally satisfied because S1 must be kept at the on-state in order to apply AC current.

This difficulty can be avoided by applying a DC voltage to the gate terminal via a resistor with extremely large resistance (R1). This resistor corresponds to the open terminals in Fig. 3. Hence, the AC voltage across R1 is the AC voltage to be measured.

Because the PCB layout of the gating circuit can affect the common source inductance, the same layout should be utilized to apply the DC voltage to the gate terminal. The most convenient method is to utilize the actual gating circuit after replacing the gate resistor by R1. This method is applicable, if the gate driver of the gating circuit has far lower output impedance than R1. This requirement is naturally satisfied for common gate drivers.

However, if the output impedance of the gate driver is not negligible compared with R1, the voltage across R1 may not follow (5), causing measurement error in the common source inductance. In this case, the gate driver should further be replaced by a parallel-connection of a DC voltage source and a decoupling capacitor. The decoupling capacitor should be disposed at the PCB pads of the gate driver so that this measurement system can form the same wiring path for the AC current as the actual gating circuit. This method can also be applicable, if no gate driver is mounted on the PCB.

C.Design of Frequency of AC current and Gate Resistance

As shown in the previous subsection, the gate resistor should be replaced by resistor R1 with large resistance so that the gating circuit can be regarded as the open circuit at the frequency of the AC current. This subsection derives required resistance for R1.

In Fig. 3(b), the wiring path between the gate and source terminals are regarded as the open circuit. However, if the DC voltage is applied via R1, the AC equivalent circuit shown in Fig. 3(b) can be modified as Fig. 4(a) (The resistance of R1 is denoted as R_1.)

Note that the impedance of the series connection of R_1, $C_{gs}+C_{gd}$, L_g, and r_g is generally far larger than that of L_s, r_s, and R_{on}. Therefore, R_1 can be approximated to have no effect on the voltage drop at L_s, r_s, and R_{on}. If the impedance of C_{gd} and C_{gs} are assumed to be far greater than R_{on}, Fig. 4(a) can be further approximated using Thevnin's thorem as Fig. 4(b). (The value of the voltage v_s can be obtained according to the same discussion as that used to derive (5).)

As can be seen in Fig. 4(b), the voltage across R1, i.e. the voltage v_g, can be measured as a result of dividing v_s by R_1, $C_{gs}+C_{gd}$, L_g, and r_g. This indicates that R_1 should be designed to be far larger than the impedance of $C_{gs}+C_{gd}$, L_g, and r_g.

However, in actual applications, accurate values of L_g and r_g may often be unknown. A convenient method to avoid this difficulty is to choose the frequency of the AC current at a frequency far lower below the parasitic LC resonance frequency of $C_{gs}+C_{gd}$ and L_g. (However, excessively low frequency may be inappropriate, because the voltage drop at the common source inductance becomes too small to ensure sufficient S/N ratio for the AC voltage measurement.) In this case, the impedance contributed by the parasitic elements, i.e. $C_{gs}+C_{gd}$, L_g, and r_g, can be commonly approximated as $1/j\omega(C_{gs}+C_{gd})$.

Now, the measurement error of the common source inductance is briefly estimated to discuss necessary resistance for R1. In order to simplify the discussion, $r_s+\alpha R_{on}$ is approximated to be small compared with the impedance of the common source inductance L_s. Then, the AC voltage drop v_s, defined in Fig. 4(b), is divided by R_1 and $1/j\omega(C_{gs}+C_{gd})$ as the phasor diagram shown in Fig. 5. The proposed measurement method estimates the voltage drop at the common source inductance as the AC voltage v_m because the component perpendicular to the AC current is calculated based on the measured AC voltage at R_1. As a result, the measurement error ε of the common source inductance can be expressed as

$$\varepsilon = \frac{|v_s| - |v_m|}{|v_s|} = \frac{\dfrac{1}{\omega^2\left(C_{gs} + C_{gd}\right)^2}}{R_1^2 + \dfrac{1}{\omega^2\left(C_{gs} + C_{gd}\right)^2}}. \tag{6}$$

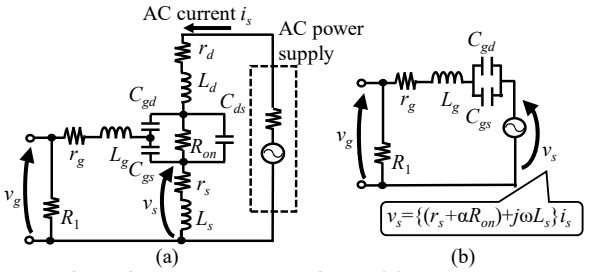


Fig. 4. Modified AC equivalent circuit of Fig. 3(b) including resistor R1.

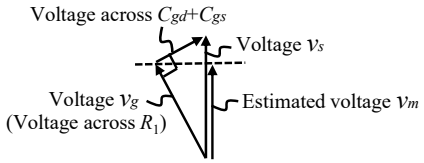


Fig. 5. Phasor diagram of the voltage induced in the common source inductance.

Therefore, R_1 should be designed to be at least 4.4 times larger than $1/\omega(C_{gs}+C_{gd})$ to keep the measurement error within 5%.

In the above discussion, R1 is assumed to be an ideal resistor. Certainly, in the actual measurement system, R1 has the stray capacitance or the stray inductance. Moreover, the voltage probe attached to R1 may add stray capacitance or parasitic input resistance in parallel to R1. However, similarly as in the above discussion, the measurement error is caused by the voltage division between the total impedance of R1 and the impedance of C_{gs}+C_{gd}. Therefore, the measurement error is scarcely affected by the stray inductance or capacitance as far as they cause minor effect on the total impedance of R1.

Certainly, the input impedance of the voltage probe may greatly affect the total impedance of R1, if R_1 is set at a resistance close to or higher than the input impedance. In this case, the measurement error becomes larger than the prediction based on (6). Therefore, if the measurement error is required to be estimated based on (6), R1 should also be far smaller than the input resistance of the voltage probe.

D. Merits

As shown in the introduction, the common source inductance has three features that cause difficulties in measurement. However, the proposed measurement method does not suffer from these features according to the following reasons.

First, the AC voltage is measured only at resistor R1 in the proposed method. Therefore, direct voltage measurement inside the semiconductor package is not required. Second, the proposed method can measure the common source inductance including the mutual inductance between the drain current path and the wiring path of the gating circuit. Third, the measurement principle of the proposed method does not utilize the parasitic LC resonance. Therefore, the common source inductance is not required to form a LC resonator consisting of a capacitor and a loop wiring path.

In addition, the proposed method has a merit that this method is applicable to an already-mounted power circuit. As discussed above, the proposed method rather utilizes the existing gate driver and gating circuit. Therefore, the measurement system can be constructed directly based on the existing power circuits as far as the AC current applied for the measurement is designed not to flow in the other part of the power circuit.

For example, if the proposed method is applied to the low-side switch of a half-bridge circuit, the high-side switch should be kept at the off-state and no circuit element should be connected to the midpoint except for the high-side and low-side switches. Similarly, if the proposed method is applied to the high-side switch, the low-side switch should be kept at the off-state, while no circuit element is connected to the midpoint except for the switches.

Besides, the proposed method has another merit that this method can be carried out using common measurement instruments for electronics engineers. Actually, a signal generator suffices to apply AC current to the drain current path; and an oscilloscope with a voltage probe and a current probe suffices to measure the AC voltage and current.

III. EXPERIMENT

Two experiments were carried out to evaluate the proposed measurement method. The first experiment verifies the proposed method by comparing the measurement result of the common source inductance with the simulation result. Then, the second experiment verifies the proposed method by inserting wires with known inductance at the common source path and comparing the measured increase in the common source inductance with this known inductance.

In these experiments, a SiC-MOSFET in TO-247 package (Cree Inc., C3M0065090D) was employed for measurement of the common source inductance. There were two reasons. 1. The first experiment required investigation of the physical package structure beneath the mold to construct the simulation model of the package. For this purpose, the comparatively large package as TO-247 was convenient for removing the mold using a handy grinder. 2. The second experiment inserted the additional wiring to the source terminal. Therefore, TO-247 package was also convenient because it has a comparatively long terminal.

As discussed in the previous section, the proposed method requires $\alpha R_{on}^2 C_{par}$ to be ignorable compared to the common source inductance. As for the device employed in this experiment, $\alpha R_{on}^2 C_{par}$ was calculated as 0.8pH, which is far smaller than the order of the common source inductance measured in this experiment.

A. Comparison with Simulation

The first experiment evaluated the common source inductance of the SiC-MOSFET using the proposed method. Then, the result was compared with the simulation to confirm appropriateness of the proposed method. The common source inductance was evaluated for two cases: 1. only a single MOSFET is mounted on a PCB without a gate driver; 2. a half-bridge circuit is mounted on a PCB along with a gating circuit. The purpose of evaluating the two cases is to show that the proposed method is applicable to a switching device of an already-mounted power circuit.

Fig. 6 and Fig. 7 show photographs, circuit diagrams, and

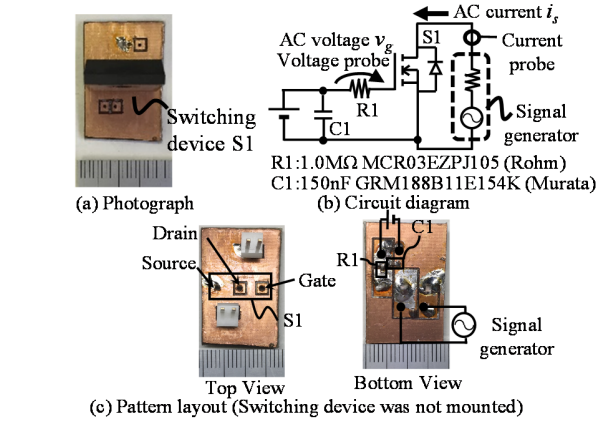


Fig. 6. Experimental PCB only with a switching device (PCB A).

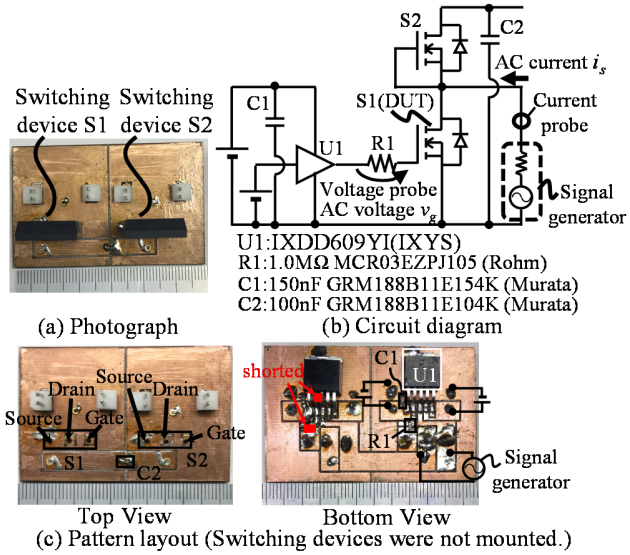


Fig. 7. Experimental PCB of a half-bridge circuit (PCB B).

TABLE I
INSTRUMENTS EMPLOYED FOR THE EXPERIMENT

Instrument	Model Number (Manufacturer)
Oscilloscope	MDO3034 (Tektronix)
Current probe	TCP305A (DC–100MHz) (Tektronix)
Passive voltage probe	TPP050B (DC–350MHz) (Tektronix)
Function generator	WF1967 (NF Corp.)

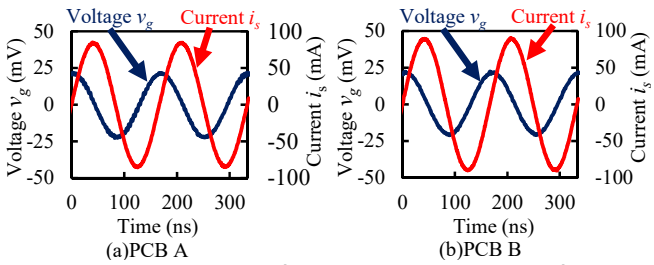


Fig. 8. Measurement results of the voltage and current waveforms.

pattern layout of two types of experimental PCBs with the switching devices under test. Fig. 6 is the PCB on which only a switching device is mounted. (Hereafter, this PCB is referred to as PCB A.) On the other hand, Fig. 7 is the PCB of a half-bridge circuit with the gating circuit. (Hereafter, this PCB is referred to as PCB B.) This experiment evaluated the common source inductance of the low-side switch. The layout near the gate and source terminals of the low-side switch was designed to have similar pattern to that of PCB A so that PCB A and PCB B have similar mutual inductance between the drain current path and the wiring path of the gating circuit. Five boards are constructed for each type of experimental PCBs to evaluate the variation of the measurement result.

The half-bridge circuit of PCB B was prepared for the proposed method. The gate and source terminals of the high-side switch was short-circuited so that this device is kept at the off-state. In addition, no circuit element was connected to the midpoint except for the high-side and low-side switches.

Table I shows the instruments for the experiment. The proposed method utilizes the phase difference between the voltage and the current. Therefore, in this experiment, the difference in the propagation delay between the current probe and the passive voltage probe was calibrated because this difference (0.45rad at 6MHz) can yield a measurement error of 10%, approximately without calibration.

The current probe was connected to the output of the signal generator to measure the drain current i_1. Certainly, in PCB B, the output of the signal generator was connected to the series connection of S2 and C2 as well as the drain and source terminals of S1. However, all of the AC current from the signal generator must flow in S1 because S2 and C2 formed the rectifying circuit and therefore S2 was naturally reverse biased. (Note that S2 was kept in the off-state.)

The voltage probe is connected to R1. Resistance R1 was set at 1.0MΩ, which is far smaller than the input impedance of the voltage probe attached to R1 and is at least 2400 times greater than $1/\omega(C_{gs}+C_{gd})$. The frequency of the AC current applied to the drain current path was ranged from 6.0MHz to 9.0MHz. The common source inductance was evaluated at 16 frequencies in order to confirm that the measurement result is not affected by the frequency.

Fig. 8 shows the current and voltage waveforms of board 1 of PCB A and PCB B measured at 6MHz. Both of the waveforms were sinusoidal. Based on the sinusoidal waveforms, i_s, v_g, and ϕ were measured. Then, the common source inductance was determined according to (1).

Fig. 9 shows the common source inductance measured for PCB A and PCB B. The results are almost constant regardless to the frequency, indicating that the proposed method is not affected by the frequency, as expected from the theory.

For each board, the average value as well as the standard deviation of the common source inductance measured at 16 frequencies was calculated. Table II shows the result. The sample standard deviation was found to be within 5% of the average value. The result supports that the proposed method can measure the common source inductance with small variation regardless to the frequency. In addition, almost the same common source inductance was obtained for PCB A and PCB B, indicating that the proposed method can be applicable to already-mounted power circuits.

Next, the standard deviation among the boards was calculated based on the common source inductance averaged over the frequency. As a result, the standard deviation was

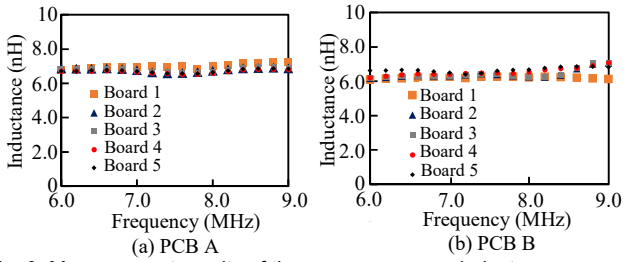


Fig. 9. Measurement results of the common source inductance.

TABLE II
AVERAGE VALUE AND STANDARD VARIATION OF THE COMMON SOURCE INDUCTANCE MEASURED AT 16 FREQUENCIES

PCB A	Average	Standard deviation	Coefficient of variation
Board 1	7.0nH	0.14nH	2.0%
Board 2	6.8nH	0.11nH	1.7%
Board 3	6.8nH	0.11nH	1.6%
Board 4	6.7nH	0.10nH	1.5%
Board 5	6.7nH	0.10nH	1.5%

PCB B	Average	Standard deviation	Coefficient of variation
Board 1	6.2nH	0.05nH	0.8%
Board 2	6.4nH	0.27nH	4.2%
Board 3	6.4nH	0.28nH	4.3%
Board 4	6.5nH	0.23nH	3.5%
Board 5	6.7nH	0.14nH	2.1%

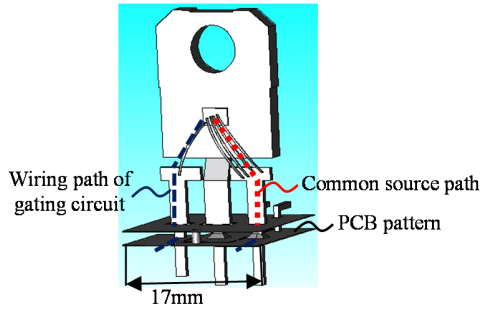


Fig. 10. Simulation model of PCB A with the semiconductor package mounted on-board.

found to be 0.12nH in PCB A and 0.17nH in PCB B, both of which is within 3% of the average common source inductance.

In order to confirm appropriateness of the measurement result, the simulation of the common source inductance was carried out based on the FEM simulation. Fig. 10 depicts the simulation model. This model consists of the wiring of the copper. The wiring pattern and thickness was modeled after those of PCB A with the semiconductor package mounted on-board. (The PCB pattern was modeled only near the package.) The package structure was constructed based on observation result of an actual switching device, from which the mold was removed using a handy grinder.

The FEM simulator was JMAG Ver. 14.1.03h. This simulator can calculate the 3-dimensional electromagnetic field when the AC current is applied to the predetermined point in the model. Based on the result, this simulator can also calculate the voltage induction at any point of conductors in the model.

As shown in the appendix, the mutual inductance between the drain current path and the wiring path of the gating circuit is equivalent to the common mode inductance. Therefore, the common source inductance was calculated based on the sum of the voltage induction in the common source path (marked by the red dotted line) and that in the wiring path in the gating circuit (marked by the blue dashed line).

According to the simulation, the common source inductance was calculated as 6.6nH at 6.0MHz, which is a similar value as the experimental results. The maximum deviation from the measurement results of PCB A (the average value over 16 frequencies and 5 boards) was found to be within 3% of the measured common source inductance. The result supports appropriateness of the proposed measurement method.

B. Estimation of Inductance of Additional Source Wiring

In the second experiment, various wires with known inductance were inserted at the source terminal of the semiconductor package. Then, increase in the common source inductance was measured using the proposed method. Then, the measurement result was compared with the known inductance to confirm appropriateness of the proposed method.

Fig. 11(a) illustrates the method to insert the wiring path at the source terminal. First, the source terminal of the switching device mounted on the experimental PCB (PCB A) was cut and a U-shaped wire was inserted to elongate the common source path. Fig. 11(b) presents a photograph of the U-shaped wires.

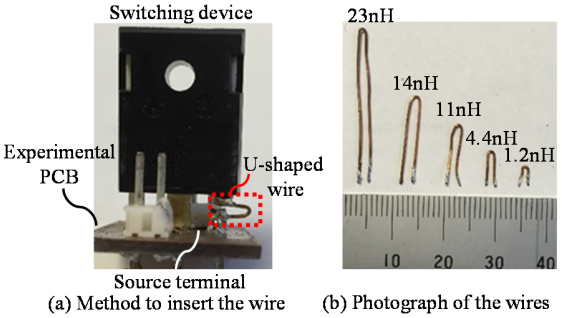
Next, the common source inductance with and without the U-shaped wires was measured using the proposed method. The measurement instruments were the same as those listed in Table I. In the measurement, the difference of the propagation delay between the current and voltage probes was calibrated similarly as in the previous subsection. Then, increase in the common source inductance was compared with the inductance of these wires, which is determined in advance using a measurement method of the stray inductance, presented in [29][30].

According to this method, the inductance of these wires was determined using the resonance frequency of the LC resonator formed with the wire. For this purpose, a ceramic capacitor with known capacitance C_a was connected between the two terminals of the U-shaped wires, as illustrated in Fig. 12. Then, the LC resonance frequency f_{res} was measured.

This frequency was measured using a signal generator with the output impedance of 50Ω and an oscilloscope, as shown in Fig. 12. The AC current was supplied using the signal generator. Then, f_{res} was searched as the frequency of the AC current that maximizes the AC voltage across the capacitor, which was measured using a voltage probe. Finally, inductance L_a of the wire can be obtained as $L_a=1/4\pi^2 f_{res}^2 C_a$. The measurement instruments, i.e. the signal generator, the oscilloscope, and the voltage probe are the same as those listed in Table I.

Fig. 13 shows the comparison result between increase in the common source inductance and the inductance of the wire measured in advance. The result indicates that the measurement result of the proposed method is consistent with the measurement method of the stray inductance of the U-shaped wire.

Consequently, both of these two experiments well supported appropriateness of the proposed measurement method.



(a) Method to insert the wire (b) Photograph of the wires

Fig. 11. U-shaped wires inserted at the source terminal of the semiconductor package mounted on PCB A.

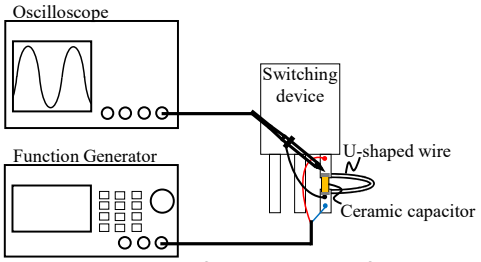


Fig. 12. Measurement system of the inductance of U-shaped wires.

IV. Conclusions

The common source inductance can be one of key designing factors for fast switching power converters of next-generation switching devices such as SiC-MOSFETs and GaN-FETs. However, measurement of the common source inductance tends to suffer from the following three features of this inductance. 1. The wiring path hidden beneath the mold of the semiconductor package significantly contributes to this inductance. 2. The mutual inductance between the gating circuit and the power circuit also contributes to this inductance. 3. This inductance cannot be defined as the stray inductance of a loop wiring path.

This paper proposed a novel measurement method that can avoid difficulties caused by these features. The proposed method is applicable to already-mounted power circuits. In addition, the proposed method offers a straightforward procedure using common measurement instruments.

This paper also presented experiments, which verified the proposed method. Consequently, the proposed method was concluded to be a promising measurement method of the common source inductance for designing power converters with next-generation switching devices.

Appendix

This appendix presents the reason why the mutual inductance between the gating circuit and the power circuit can appear as the common source inductance through constructing the AC equivalent circuit model for the switching device and the gating circuit. For convenience, this appendix bases the discussion on a simple circuit model of a switching device and a gate driver, as shown in Fig. 14(a).

The gate driver is generally composed as a half-bridge circuit that connects the output to the power supply of the gate driver

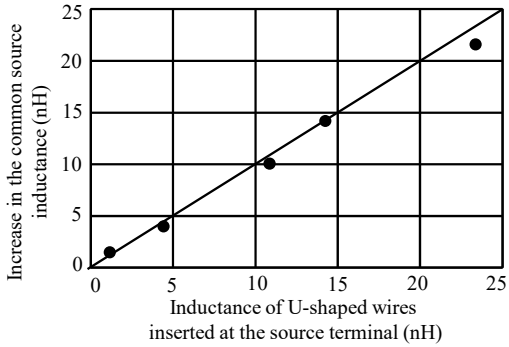


Fig. 13. Dependence of the measured increase in the common source inductance on the inductance of U-shaped wires.

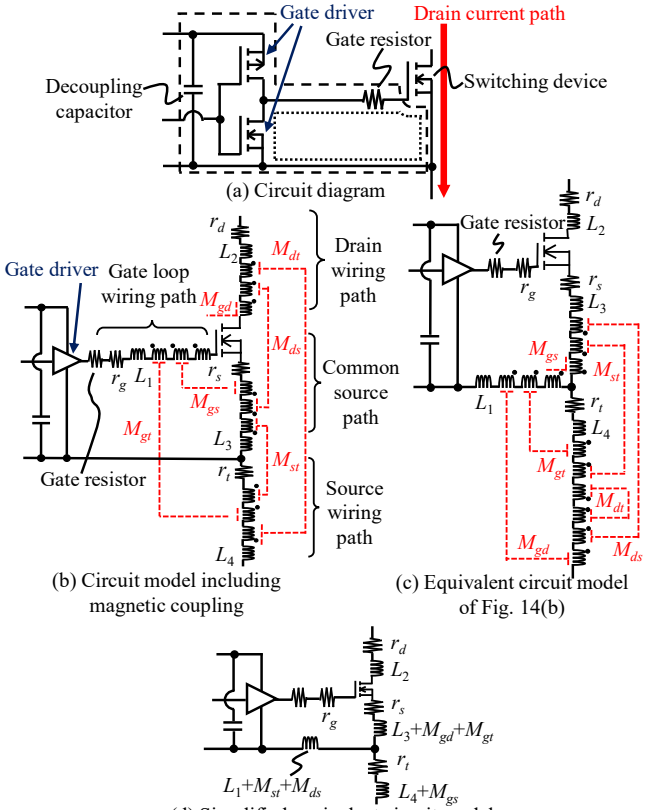


Fig. 14. Simple circuit model of a switching device with a gate driver.

in the on-state and to the ground of the gate driver in the off-state. Therefore, the gate driver forms a loop wiring path marked by the dashed line in the on-state and that marked by the dotted line in the off-state.

Now, the magnetic coupling is considered between these loop wiring paths and the drain current path, i.e. the current path of the drain current flowing from the drain terminal to the source terminal. For convenience, the magnetic coupling is approximated to be the same regardless to the on-state or the off-state. In order to construct the AC equivalent circuit model, the magnetic coupling is decomposed into the magnetic couplings among 4 wirings: the gate loop wiring path, the common source path, the drain wiring path, and the source wiring path. Then, these magnetic couplings were expressed using 6 virtual transformers to obtain the AC circuit model as shown in Fig. 14(b), where L_1, L_2, L_3, L_4 are the leakage

inductance and r_g, r_s, r_d, r_t are the parasitic resistance.

Next, Fig. 14(b) is transformed into an equivalent circuit to simplify the model. Note that the current of the drain wiring path is identical to that of the source wiring path. Therefore, the magnetic couplings related to the drain wiring path can be regarded to be equivalent to those related to the source wiring path, as far as the electric interference of the drain current to the gating circuit is discussed. In addition, in the AC equivalent circuit model, the magnetic components on the gate loop wiring path can be equivalently moved toward the source terminal. As a result, Fig. 14(b) can be simplified as Fig. 14(c).

Then, each of these virtual transformers are replaced by T-shaped equivalent circuit. As a result, we obtain the final equivalent circuit as shown in Fig. 14(d). The result indicates that the mutual inductance between the gating circuit and the power circuit, i.e. M_{gd} and M_{gt} appears as the equivalent common source inductance. In addition, the common source inductance appeared in Fig. 14(d) is different from the self-inductance of the common source path. Actually, the common source inductance appeared in Fig. 14(d) is $L_3+M_{gd}+M_{gt}$, whereas the self-inductance is $L_3+M_{ds}+M_{st}+M_{gs}$.

Again, moving the inductance $L_1+M_{st}+M_{ds}$ on the gate loop wiring path toward the gate terminal yields the equivalent circuit model presented in Fig. 3(a).

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